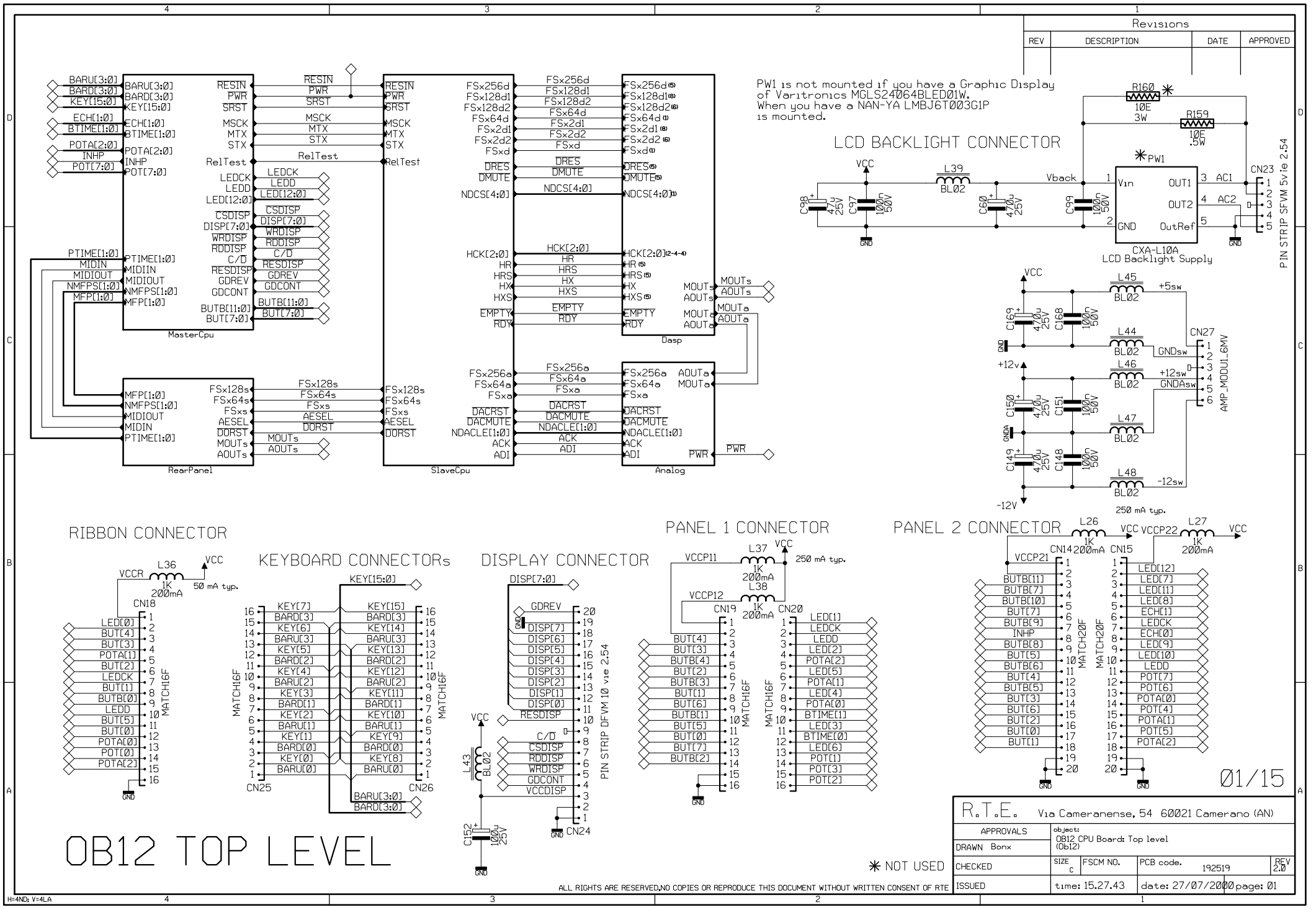
Oberheim

Manuale di Servizio - Service Manual
Schaltplan - Schéma Technique

OB12

Z-Domain Synthesis



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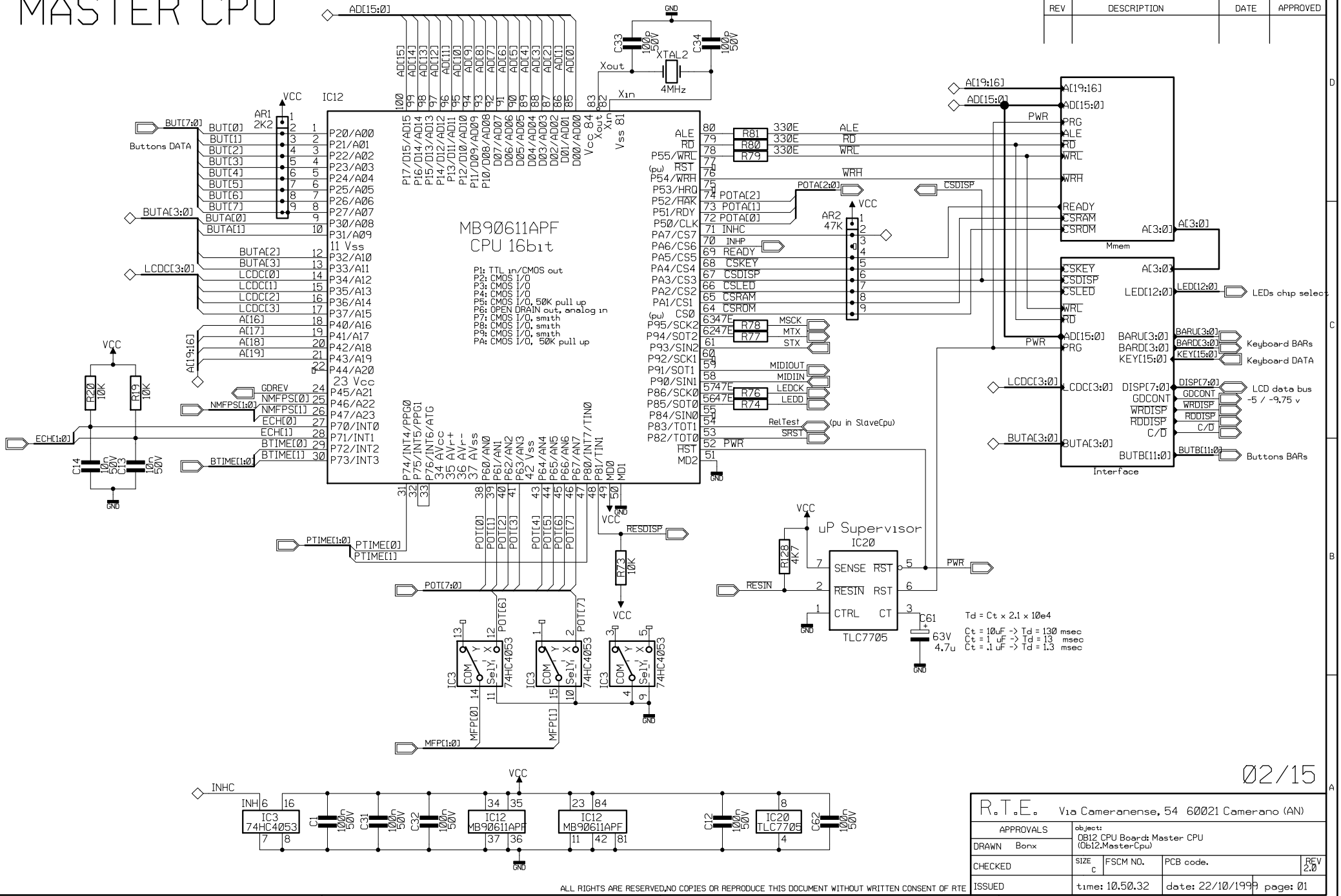
MASTER CPU
Revisions
REV
DESCRIPTION
DATE
APPROVED
MB90611APF
CPU 16bit
P1: TTL in/CMOS out
P2: CMOS I/O
P3: CMOS I/O
P4: CMOS I/O
P5: CMOS I/O, 50K pull up
P6: OPEN DRAIN out, analog in
P7: CMOS I/O, smith
P8: CMOS I/O, smith
P9: CMOS I/O, smith
PA: CMOS I/O, 50K pull up
IC12
AR1
2K2
Buttons DATA
AR2
47K
XTAL2
4MHz
Mmem
Interface
LEDs chip select
Keyboard BARs
Keyboard DATA
LCD data bus
-5 / -9.75 v
Buttons BARs
uP Supervisor
IC20
TLC7705
Td = Ct x 2.1 x 10e4
Ct = 10uF -> Td = 130 msec
Ct = 1 uF -> Td = 13 msec
Ct = .1 uF -> Td = 1.3 msec
IC3
74HC4053
IC12
MB90611APF
IC20
TLC7705
02/15
R.T.E. Via Cameranense, 54 60021 Camerano (AN)
APPROVALS
DRAWN Bonx
CHECKED
ISSUED
object:
OB12 CPU Board: Master CPU
(Ob12.MasterCpu)
SIZE C
FSCM NO.
PCB code.
REV 2.0
time: 10.50.32
date: 22/10/1999
page: 01
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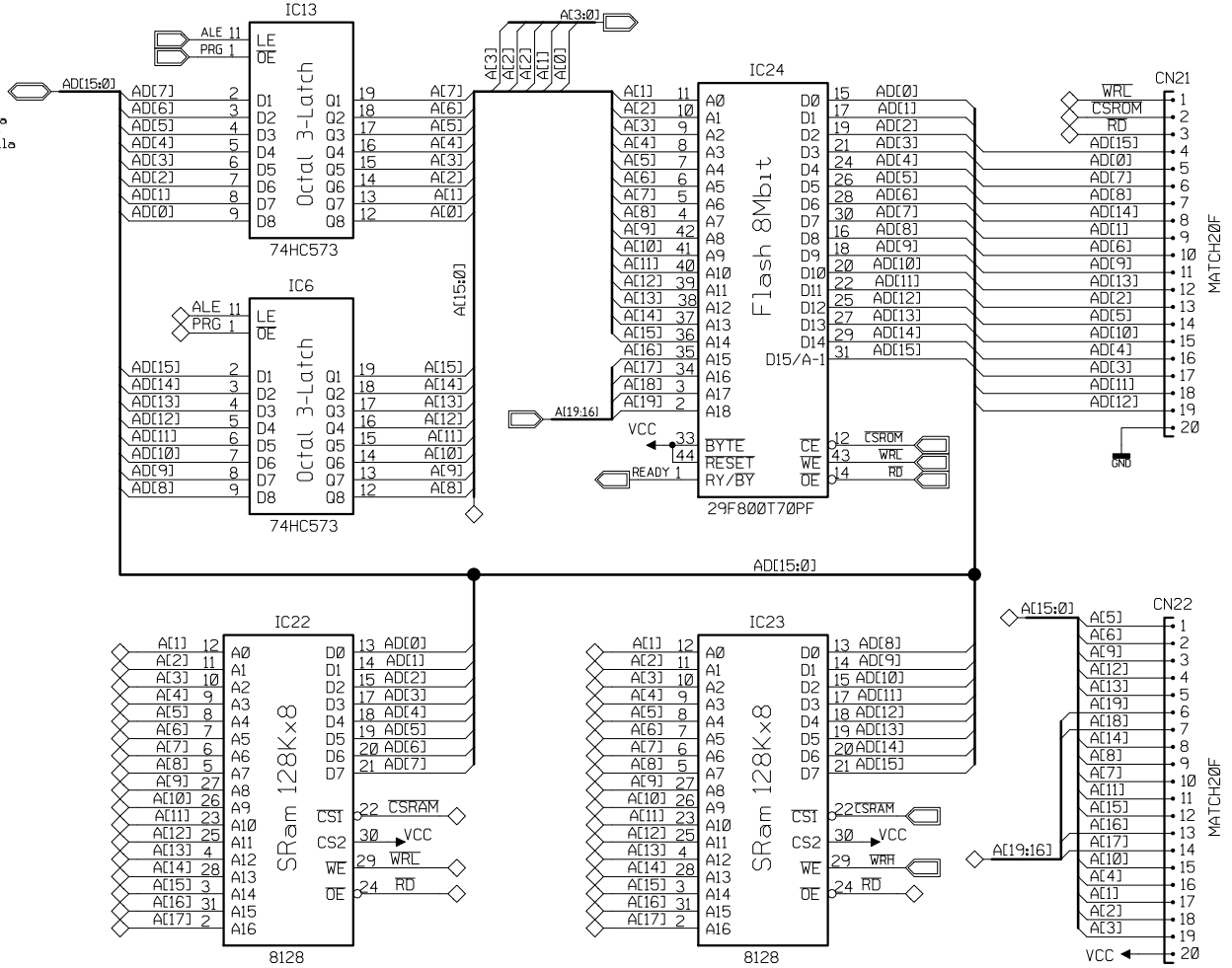
H=4ND; V=4LA

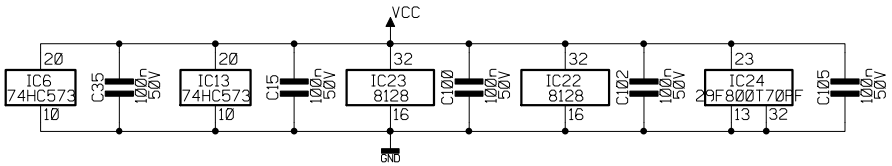
Revisions			
REV	DESCRIPTION	DATE	APPROVED

Le resistenze du PU sul bus AD[15:0] sono state rimosse dopo la verifica della procedura di programmazione della flash e del corretto funzionamento della CPU.



CS0: ROM addressing space FFFFFF-F00000;
20 bit address -> 1 Mbyte;
A0 not connected because of 16 bit data addressing;

CS1: RAM addressing space EFFFFF-E00000;
20 bit address -> 1 Mbyte;
A0 not connected because of 16 bit data addressing;
256 Kbyte on board -> E1FFFF-E00000 RAM addressing space used;



03/15

MASTER MEMORY

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Master CPU's memory (Ob12.MasterCpu.Mmem)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 12.00.33	date: 11/01/2000	page: 01

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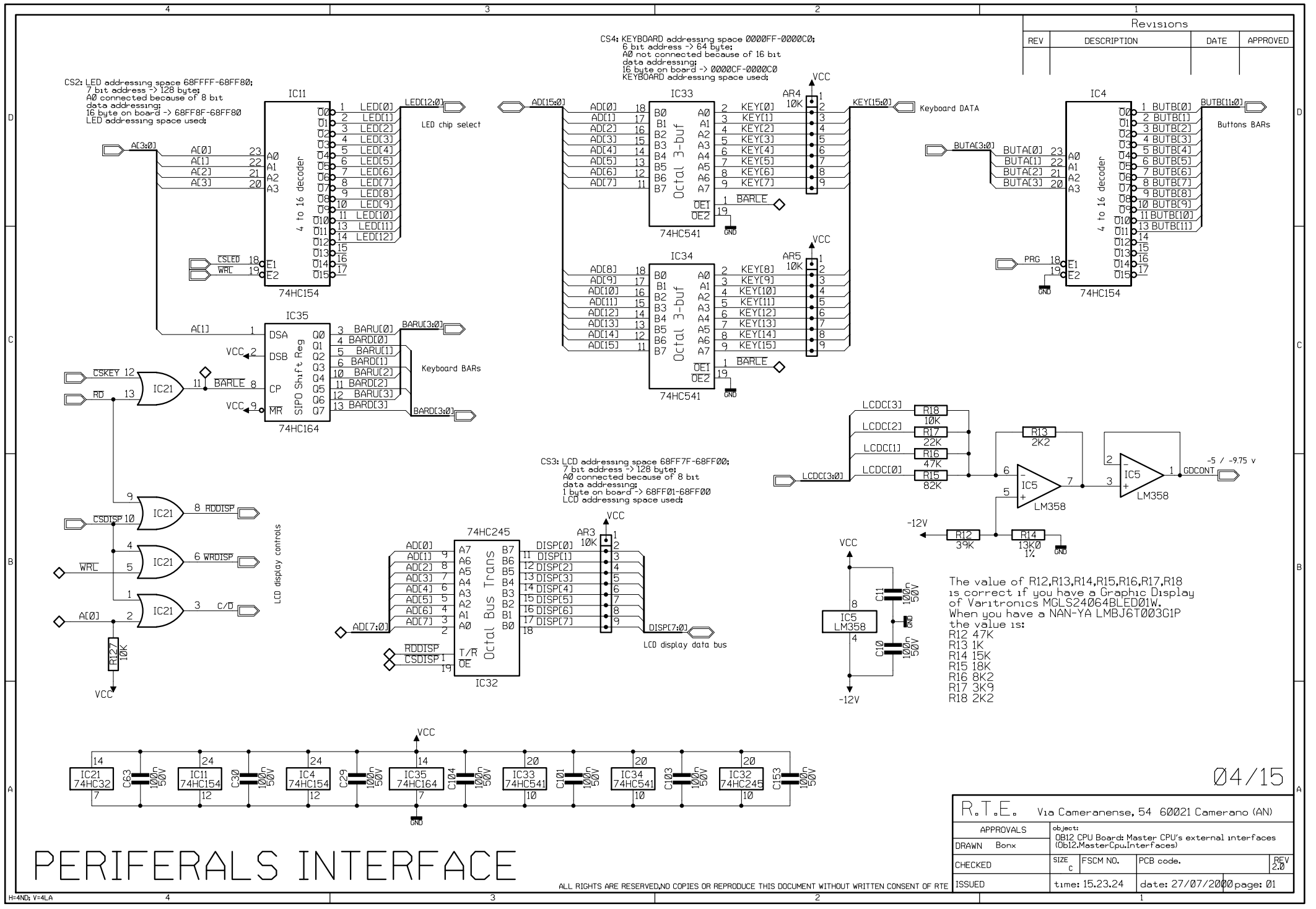
H=4ND; V=4LA


Revisions
REV
DESCRIPTION
DATE
APPROVED
CS2: LED addressing space 68FFFF-68FF80;
7 bit address -> 128 byte;
A0 connected because of 8 bit
data addressing;
16 byte on board -> 68FF8F-68FF80
LED addressing space used:
IC11
4 to 16 decoder
74HC154
LED[12:0]
LED chip select
CSLED
WRL
CS4: KEYBOARD addressing space 0000FF-0000C0;
6 bit address -> 64 byte;
A0 not connected because of 16 bit
data addressing;
16 byte on board -> 0000CF-0000C0
KEYBOARD addressing space used:
IC33
Octal 3-buf
74HC541
AR4 10K
KEY[15:0]
Keyboard DATA
IC34
AR5 10K
IC4
BUTA[3:0]
BUTB[11:0]
Buttons BARs
PRG
IC35
SIPO Shift Reg
74HC164
BARU[3:0]
BARD[3:0]
Keyboard BARs
CSKEY
RD
IC21
BARLE
CS3: LCD addressing space 68FF7F-68FF00;
7 bit address -> 128 byte;
A0 connected because of 8 bit
data addressing;
1 byte on board -> 68FF01-68FF00
LCD addressing space used:
74HC245
Octal Bus Trans
IC32
AR3 10K
DISP[7:0]
LCD display data bus
RDDISP
CSDISP
WRDISP
C/D
LCD display controls
LCDC[3:0]
R18 10K
R17 22K
R16 47K
R15 82K
R13 2K2
R12 39K
R14 13K0 1%
IC5 LM358
-5 / -9.75 v
GDCONT
-12V
VCC
GND
The value of R12,R13,R14,R15,R16,R17,R18
is correct if you have a Graphic Display
of Varitronics MGLS24064BLED01W.
When you have a NAN-YA LMBJ6T003G1P
the value is:
R12 47K
R13 1K
R14 15K
R15 18K
R16 8K2
R17 3K9
R18 2K2
C63 100n 50V
C30 100n 50V
C29 100n 50V
C104 100n 50V
C101 100n 50V
C103 100n 50V
C153 100n 50V
C11 100n 50V
C10 100n 50V
04/15
PERIFERALS INTERFACE
R.T.E. Via Cameranense, 54 60021 Camerano (AN)
APPROVALS
DRAWN Bonx
CHECKED
ISSUED
object:
OB12 CPU Board: Master CPU's external interfaces
(Ob12.MasterCpu.Interfaces)
SIZE C
FSCM NO.
PCB code.
REV 2.0
time: 15.23.24
date: 27/07/2000
page: 01
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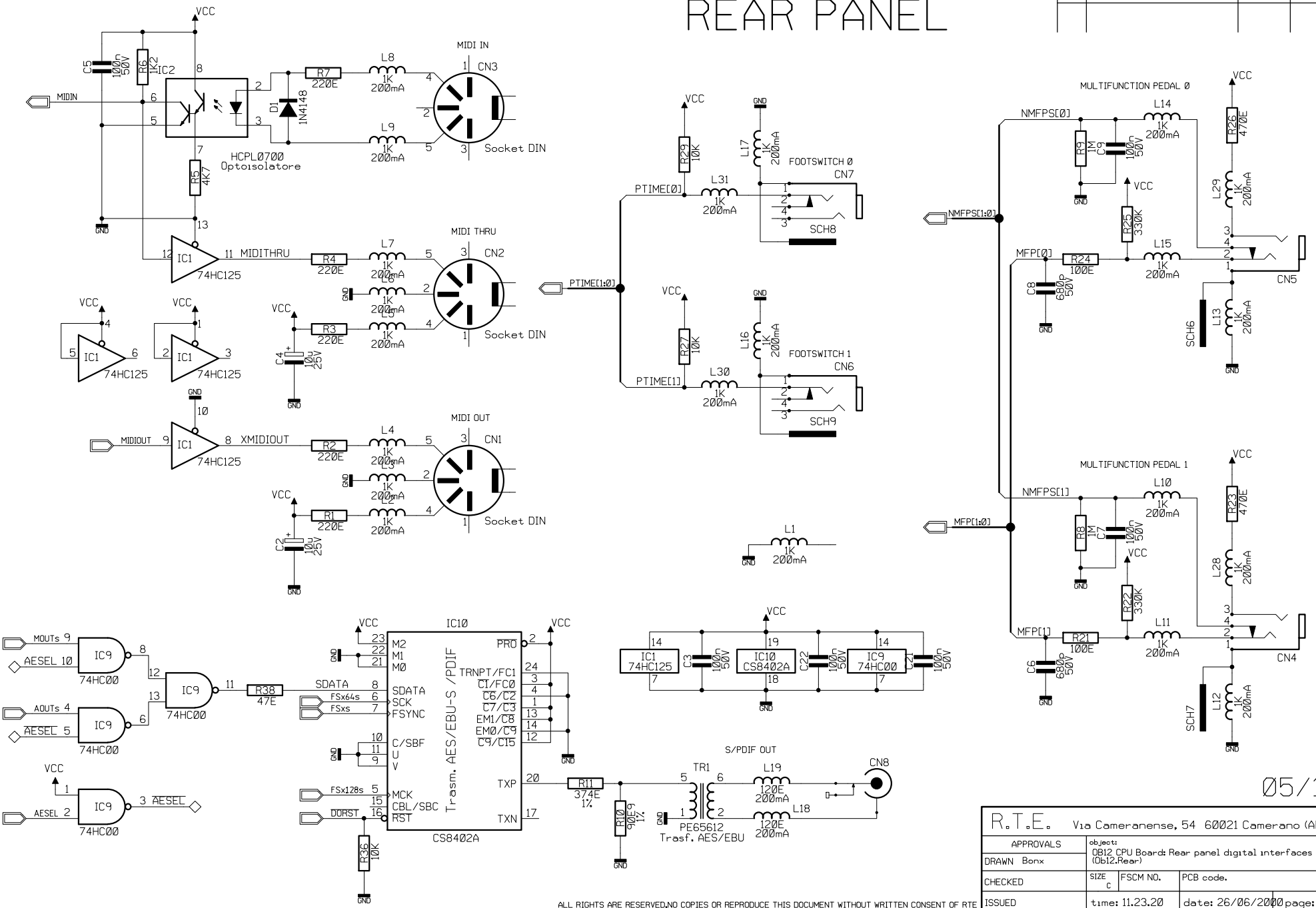
REAR PANEL

Revisions			
REV	DESCRIPTION	DATE	APPROVED



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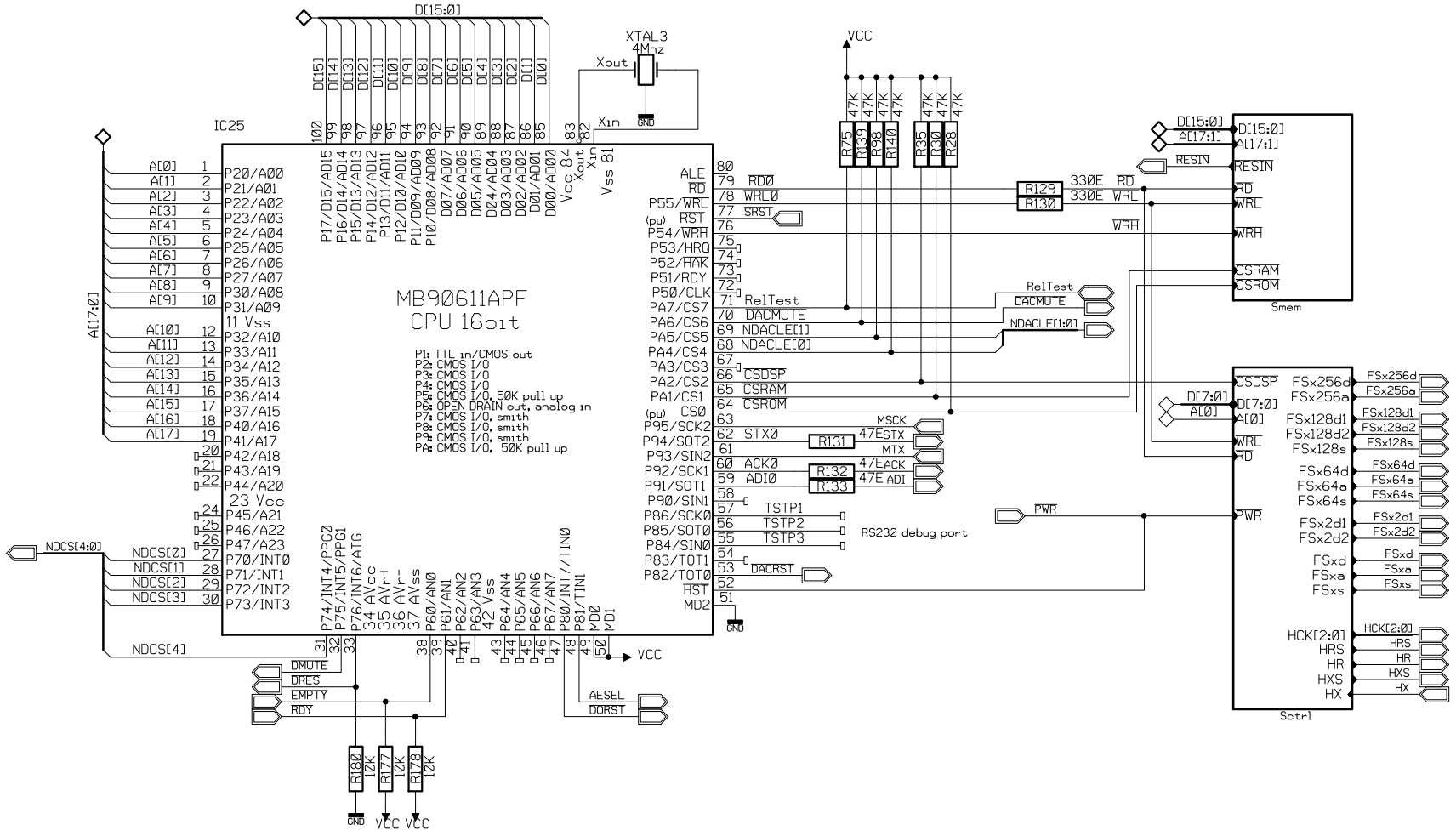
R.T.E.	Via Cameranense, 54 60021 Camerano (AN)		
APPROVALS	object: OB12 CPU Board: Rear panel digital interfaces (Ob12.Rear)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 11.23.20	date: 26/06/2000	page: 01

05/15

H=4ND; V=4LA

SLAVE CPU

Revisions			
REV	DESCRIPTION	DATE	APPROVED



06/15

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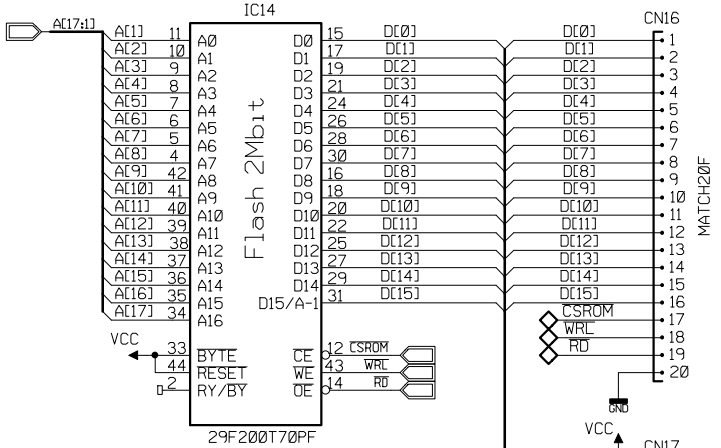
R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Slave CPU (Ob12.SlaveCpu)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 10.09.28		date: 03/11/1999 page: 01

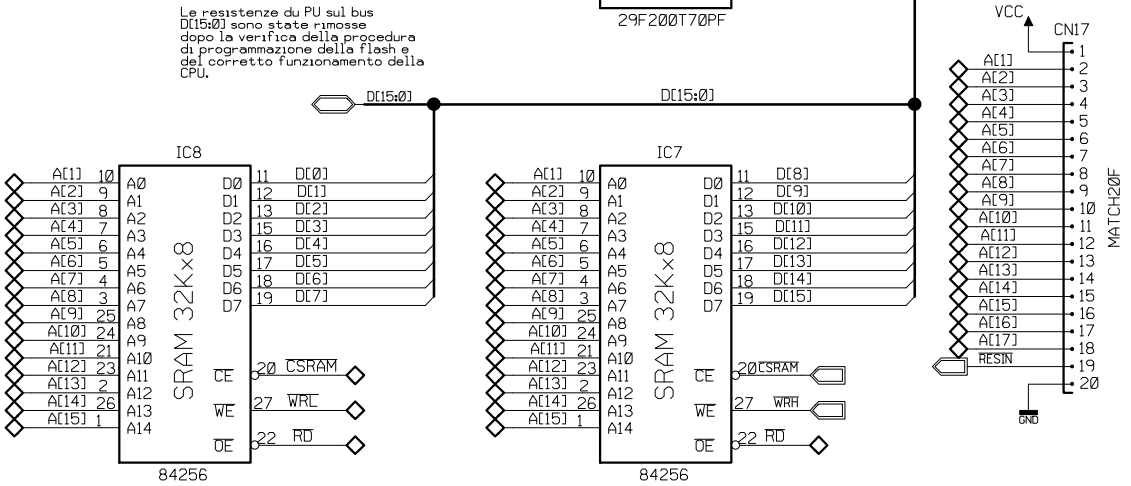
H=4ND; V=4LA

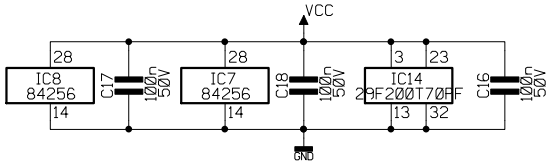
SLAVE MEMORY

Revisions			
REV	DESCRIPTION	DATE	APPROVED



Le resistenze du PU sul bus D[15:0] sono state rimosse dopo la verifica della procedura di programmazione della flash e del corretto funzionamento della CPU.





07/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Slave CPU's memory (Ob12.SlaveCpu.Smem)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 14.35.02	date: 16/09/1999	page: 01

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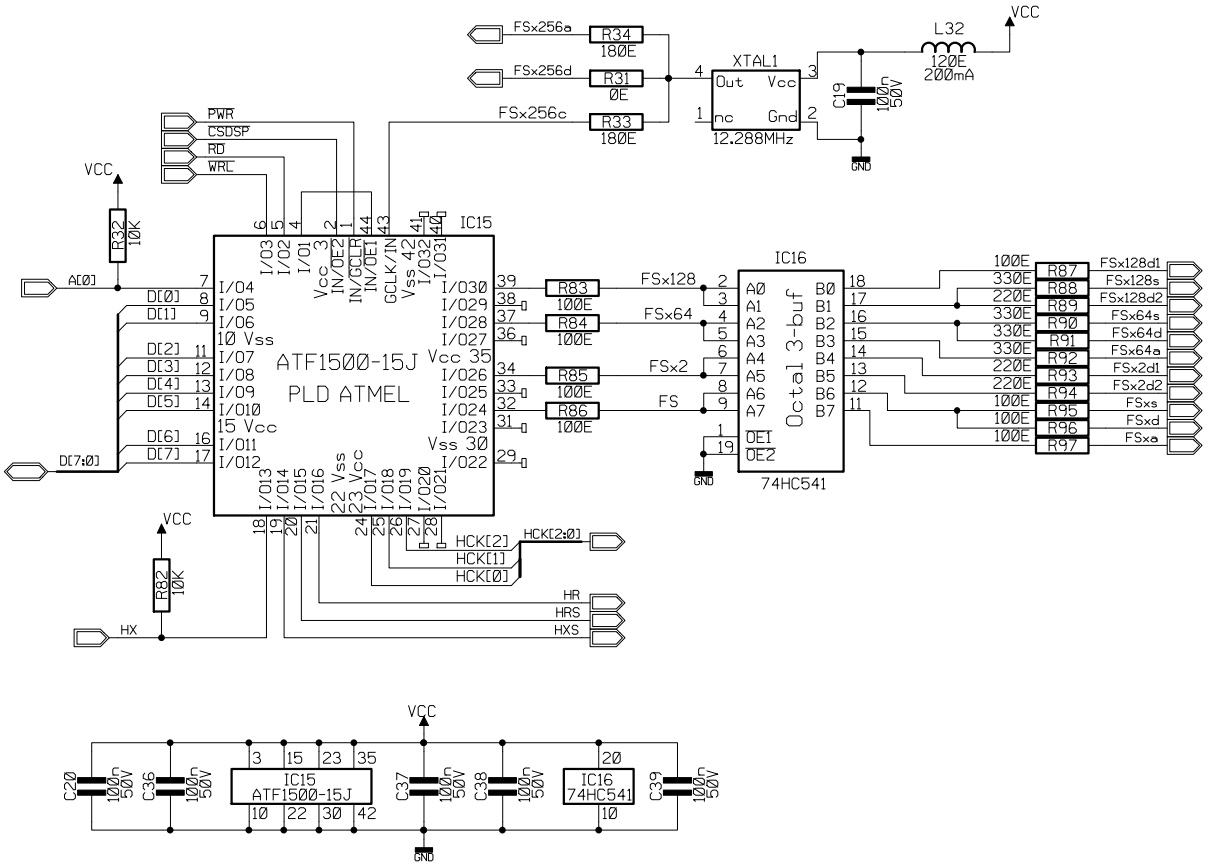
DASPs CONTROL

Revisions			
REV	DESCRIPTION	DATE	APPROVED



Ø8/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Audio generator's Slave interface (Ob12.SlaveCpu.Sctrl)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.Ø
ISSUED	time: 12.03.23	date: 11/01/2000	page: 01

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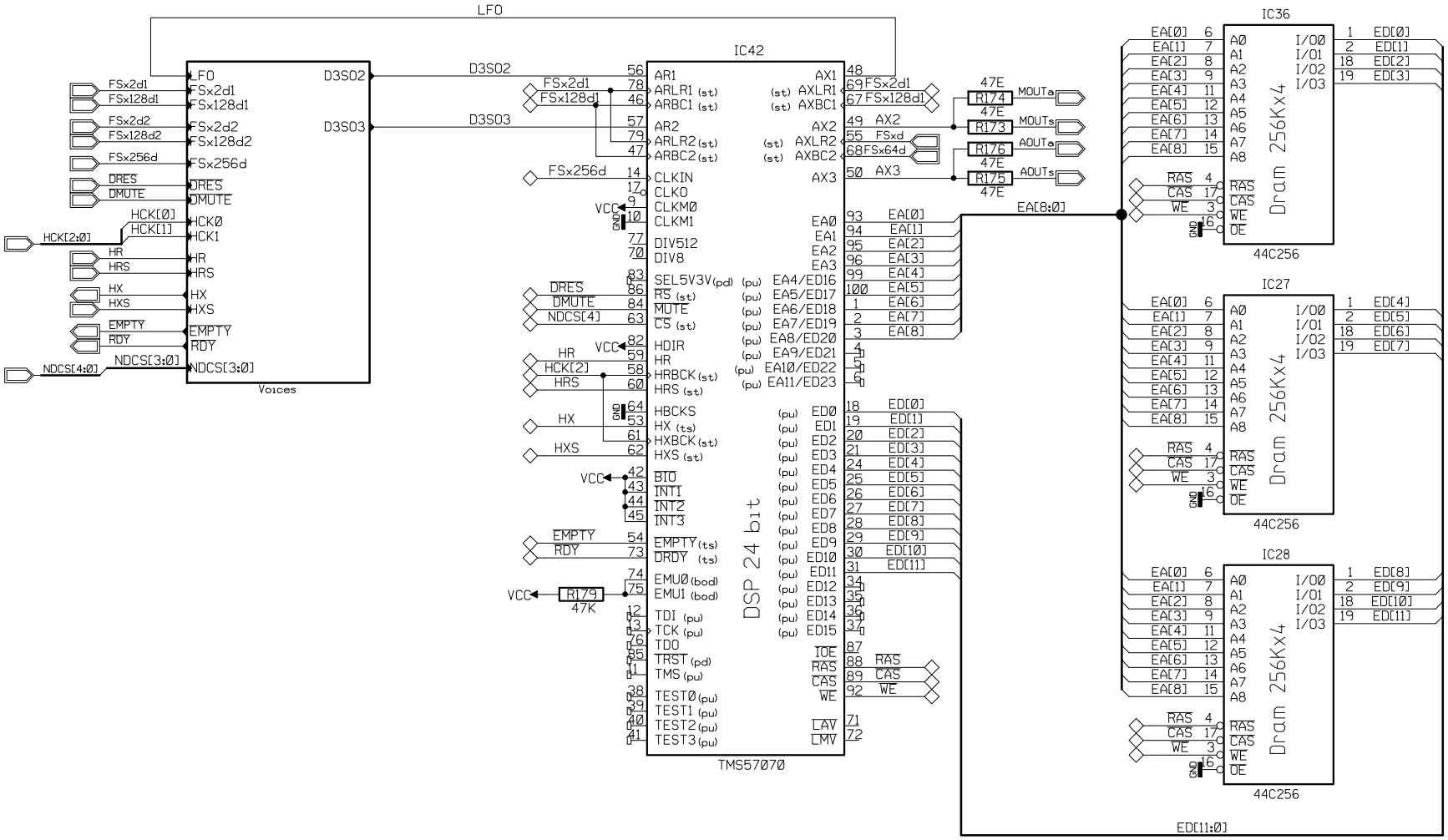
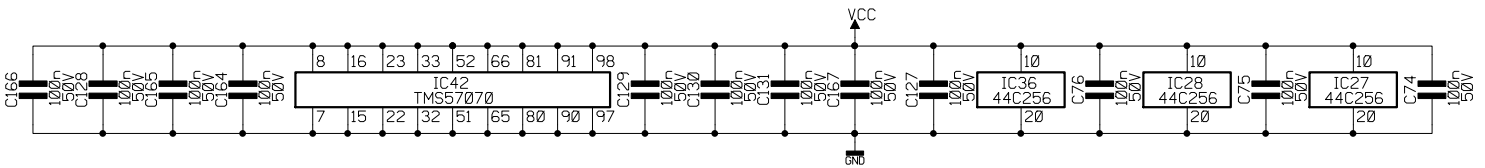
Revisions			
REV	DESCRIPTION	DATE	APPROVED

DASP[3:0] VOICEs GENERATOR

DASP[4] LFO & EFFECT GENERATOR





09/15

R.T.E.	Via Cameranense, 54 60021 Camerano (AN)		
APPROVALS	object: OB12 CPU Board: Audio generator (Ob12.Dasp)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 16.45.51	date: 07/12/1999	page: 01

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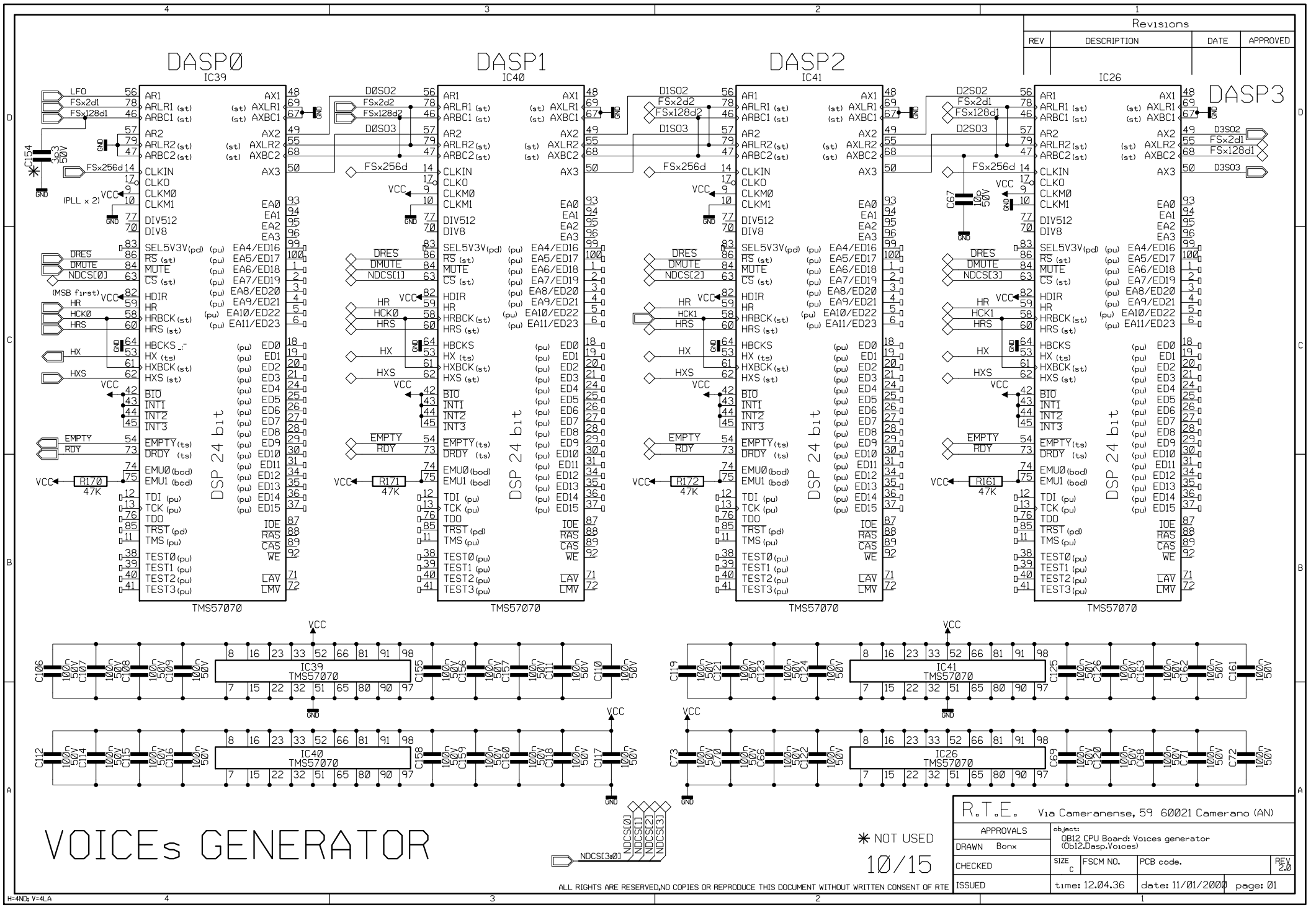
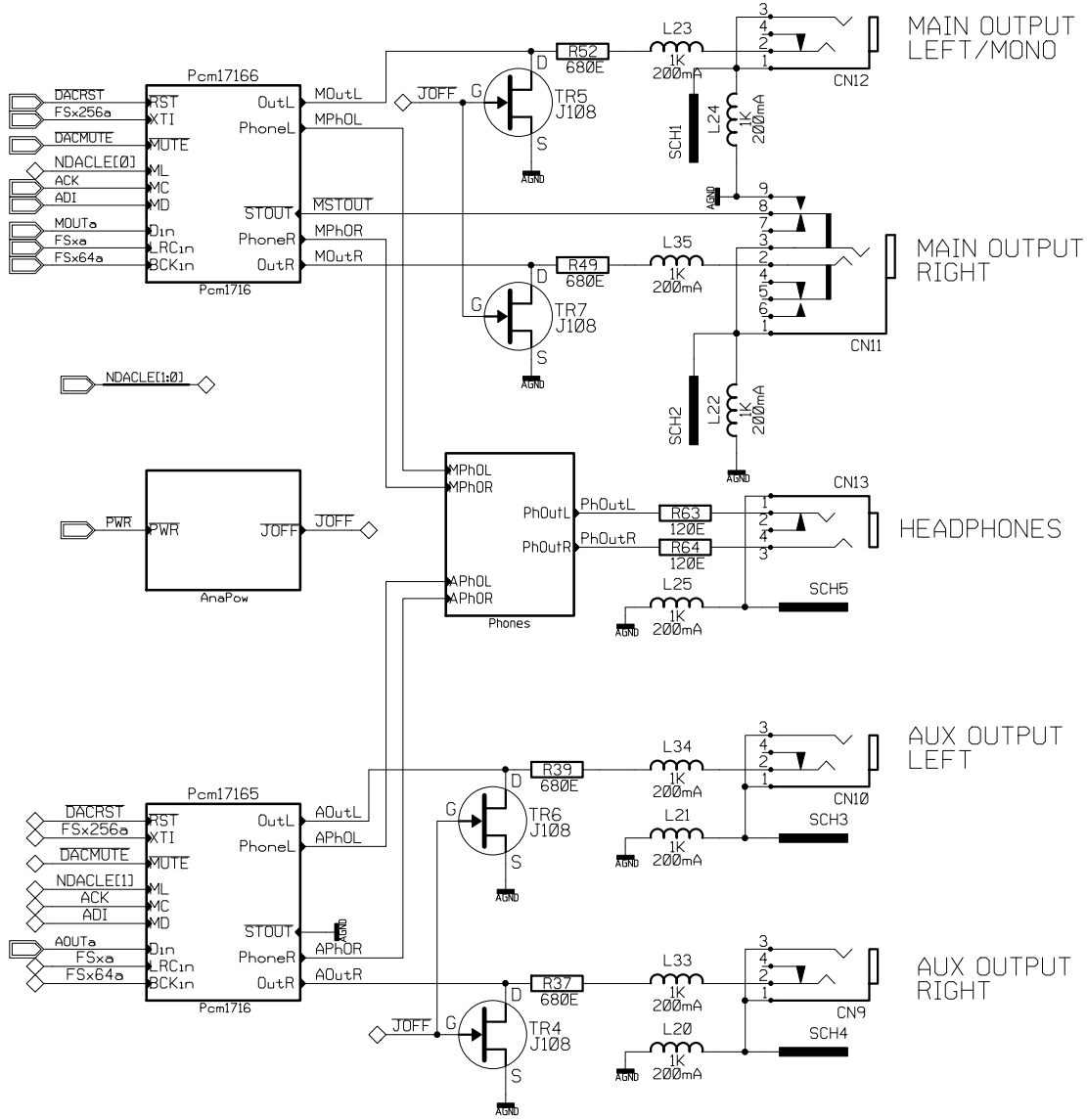


Revisions			
REV	DESCRIPTION	DATE	APPROVED

APPROVALS	object: OB12 CPU Board: Voices generator (Ob12.Dasp.Voices)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 12.04.36	date: 11/01/2000	page: 01

ANALOG OUTPUTs

Revisions			
REV	DESCRIPTION	DATE	APPROVED



11/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Analog circuits (Ob12.Analog)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 15.40.22	date: 07/12/1999	page: 01

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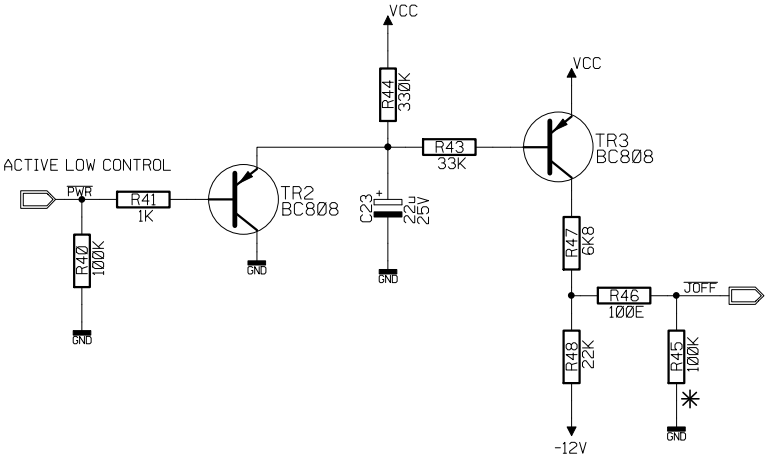
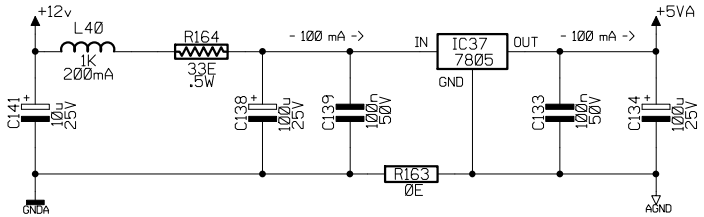
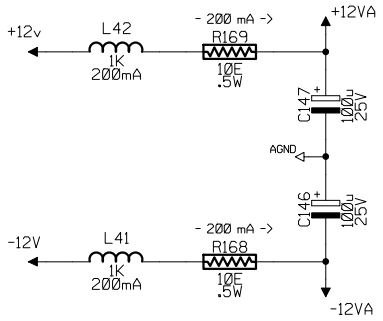
H=4ND; V=4LA

ANALOG POWER SUPPLY

Revisions			
REV	DESCRIPTION	DATE	APPROVED







12/15

✳ NOT USED

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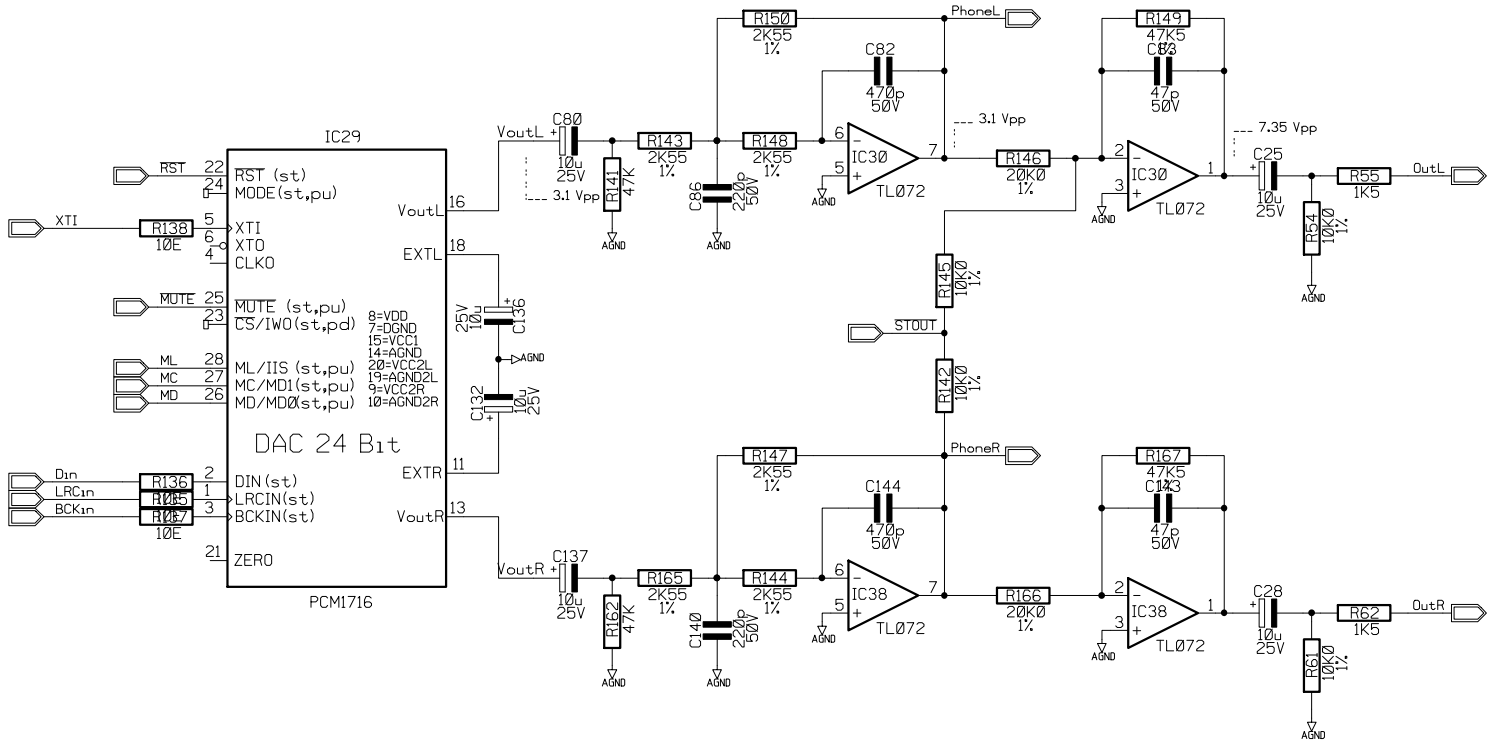
R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Analog circuit's power supply (Ob12.Analog.AnaPow)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 16.47.27	date: 07/12/1999	page: 01

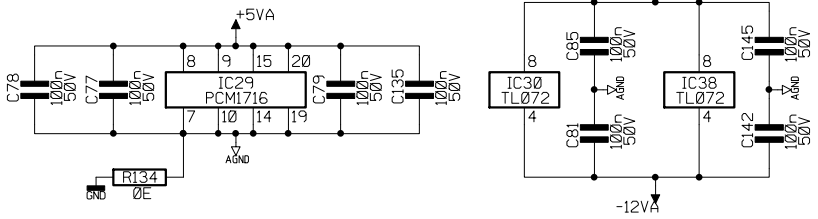
H=4ND; V=4LA

OUTPUT STEREO CHANNEL

Revisions			
REV	DESCRIPTION	DATE	APPROVED

Ft1 = 47.0 KHz; G = 1;
Ft2 = 70.5 KHz; G = 2.37;
Ft = 36.0 KHz; G = 2.37 (7.5 dB);





1 /15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: D to A conversion stereo channel (Ob12.Analog.Pcm1716)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 10.42.53	date: 22/10/1999	page: 01

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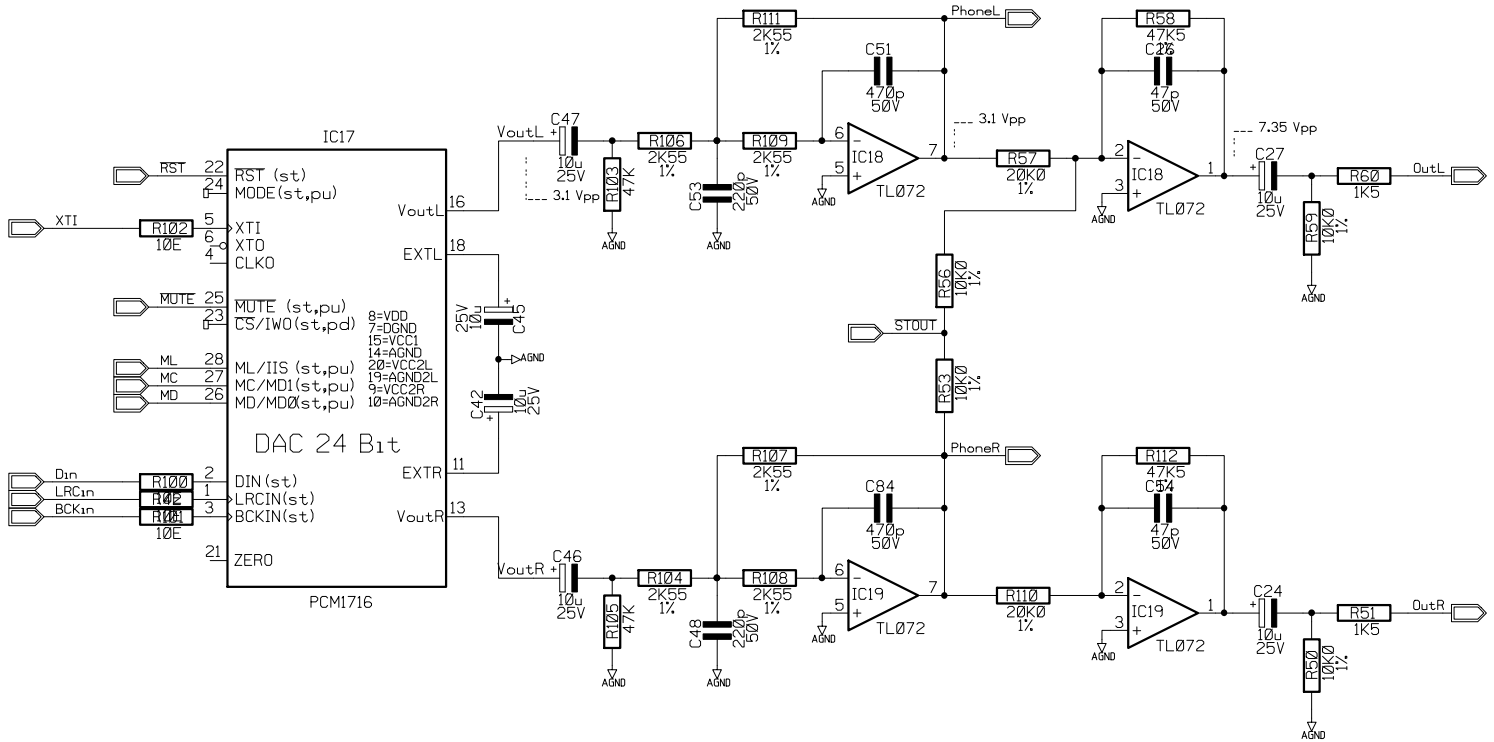
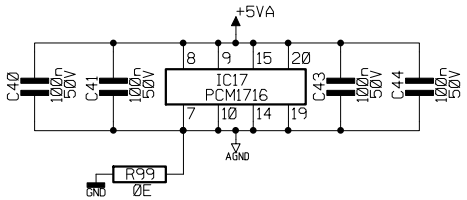
H=4ND; V=4LA

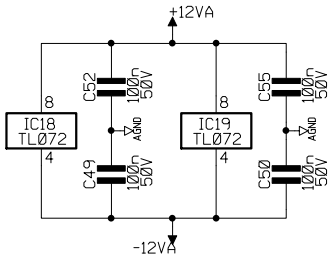
OUTPUT STEREO CHANNEL

Revisions			
REV	DESCRIPTION	DATE	APPROVED

Ft1 = 47.Ø KHz; G = 1;
Ft2 = 70.5 KHz; G = 2.37;
Ft = 36.Ø KHz; G = 2.37 (7.5 dB);







1 /15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: D to A conversion stereo channel (Ob12.Analog.Pcm1716)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.Ø
ISSUED	time: 10.42.53	date: 22/10/1999	page: Ø1

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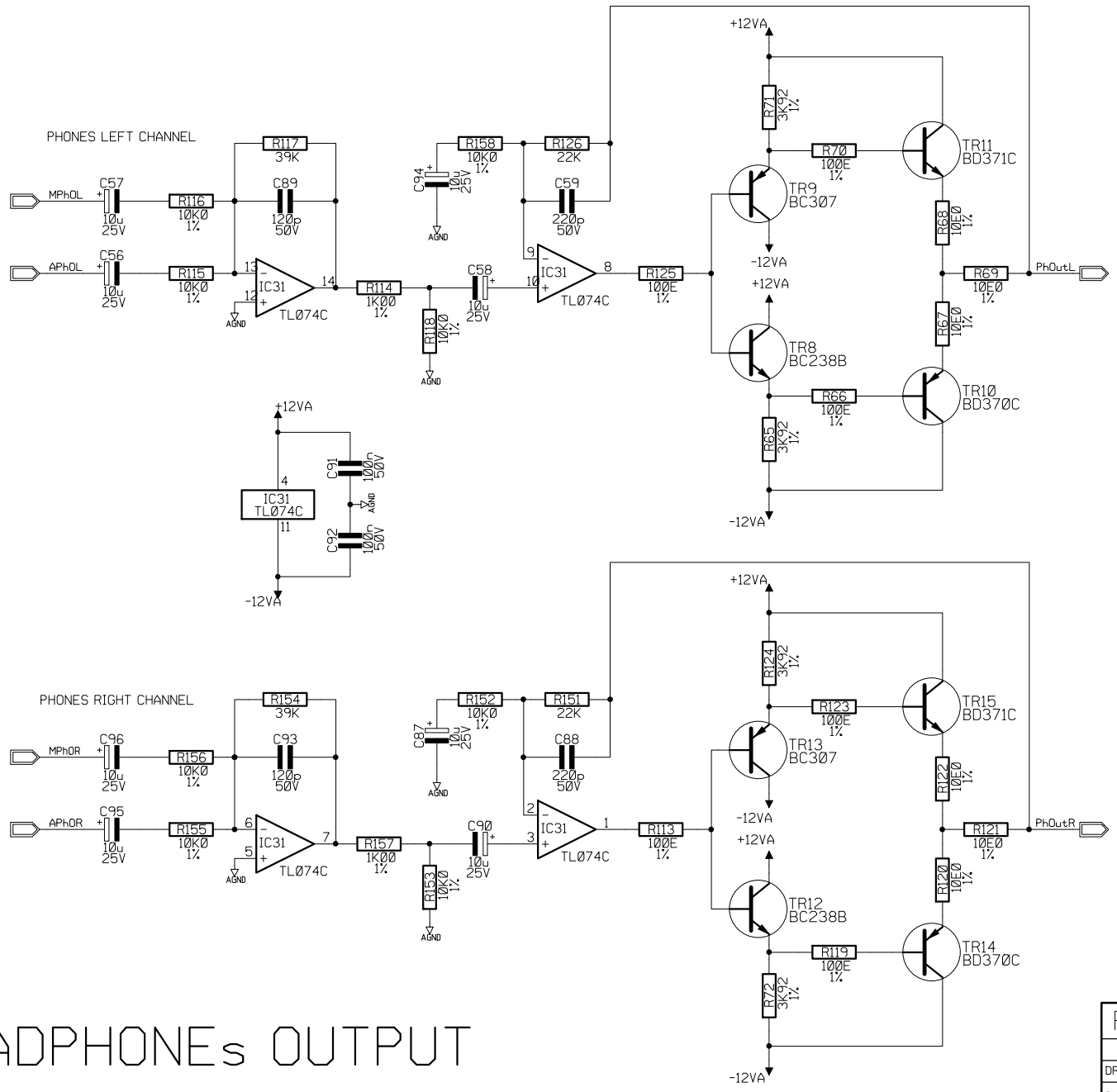
H=4ND; V=4LA



HEADPHONEs OUTPUT

Revisions			
REV	DESCRIPTION	DATE	APPROVED

15/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: HeadPhones Output (Ob12.Analog.Phones)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 09.17.53	date: 27/06/2000	page: 01

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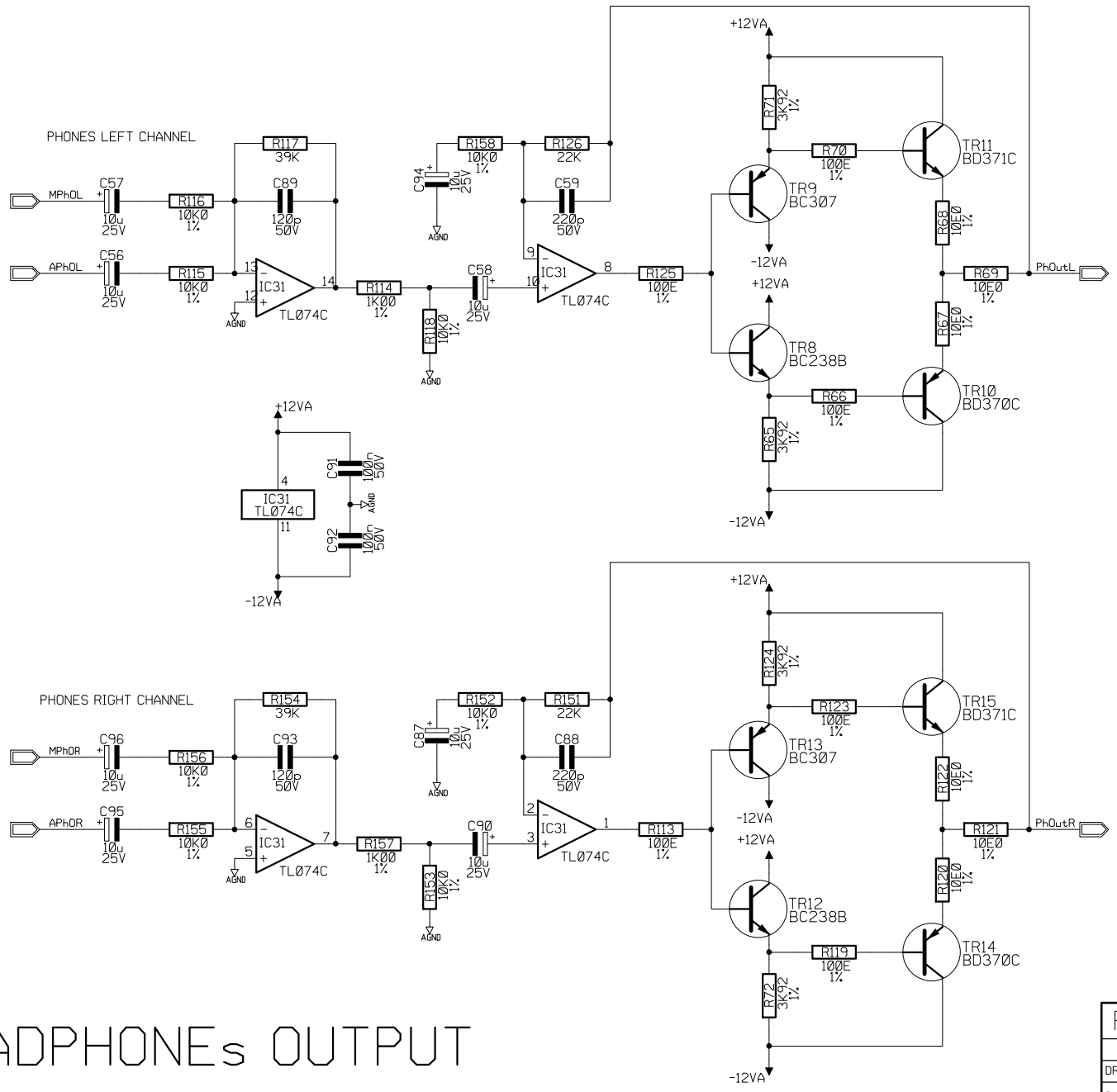
H=4ND; V=4LA



HEADPHONEs OUTPUT

Revisions			
REV	DESCRIPTION	DATE	APPROVED

15/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: HeadPhones Output (Ob12.Analog.Phones)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. REV 2.0
ISSUED	time: 11.07.43	date: 2000.06.27	page: 01

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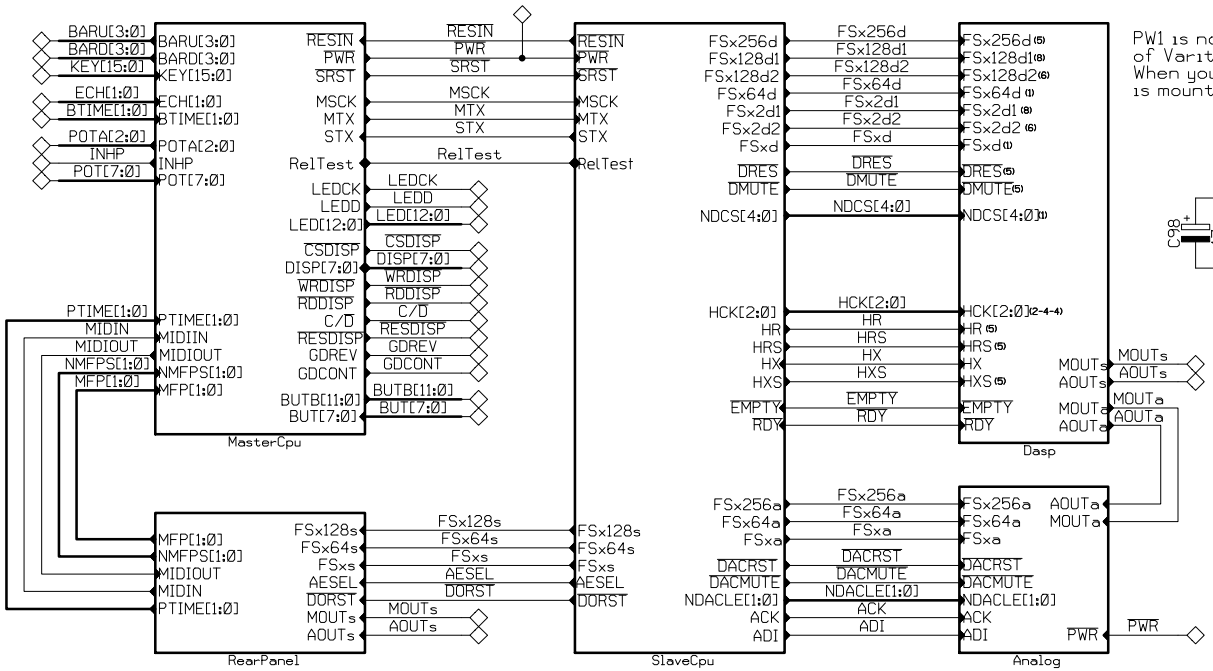
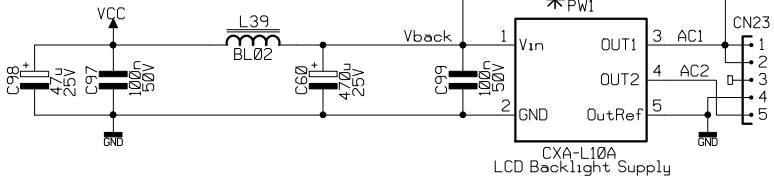
H=4ND; V=4LA

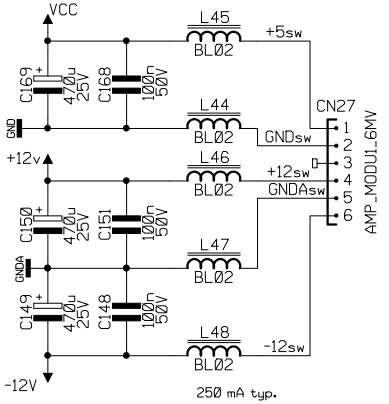
OB12 TOP LEVEL



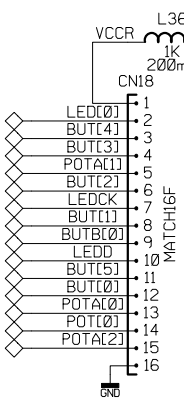
PW1 is not mounted if you have a Graphic Display of Varitronics MGLS24064BLED01W. When you have a NAN-YA LMBJ6T003G1P is mounted.

LCD BACKLIGHT CONNECTOR

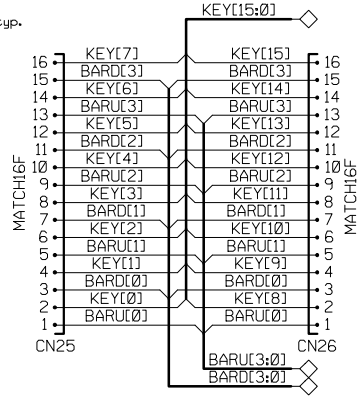




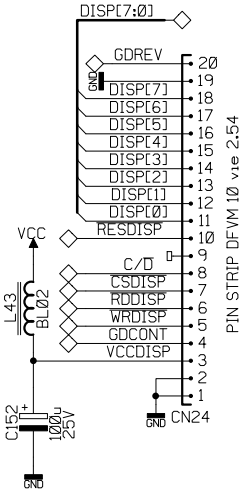
RIBBON CONNECTOR



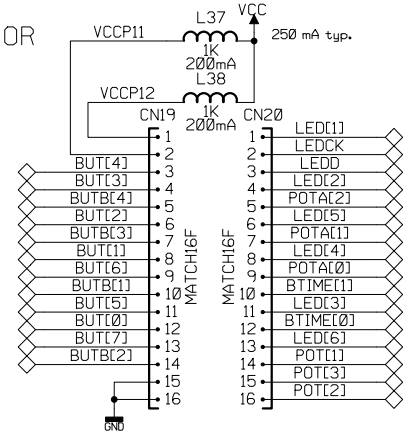
KEYBOARD CONNECTORs



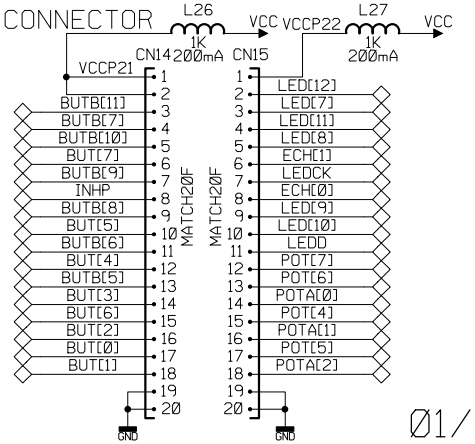
DISPLAY CONNECTOR



PANEL 1 CONNECTOR



PANEL 2 CONNECTOR



01/15

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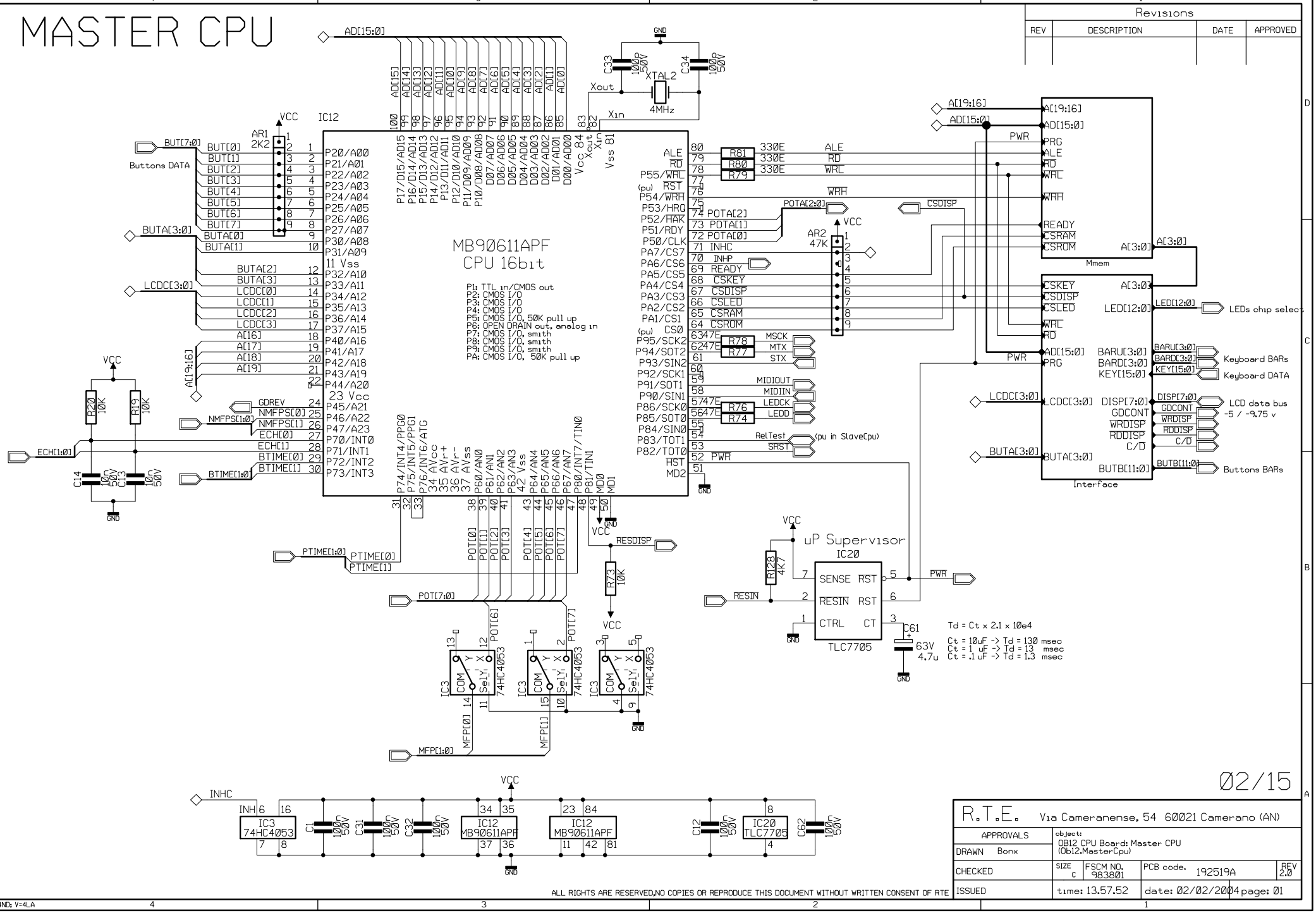
Revisions

REV	DESCRIPTION	DATE	APPROVED

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Top level (Ob12)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. 192519A REV 2.0
ISSUED	time: 10.17.56		date: 01/04/2004 page: 01

H=4ND; V=4LA

MASTER CPU



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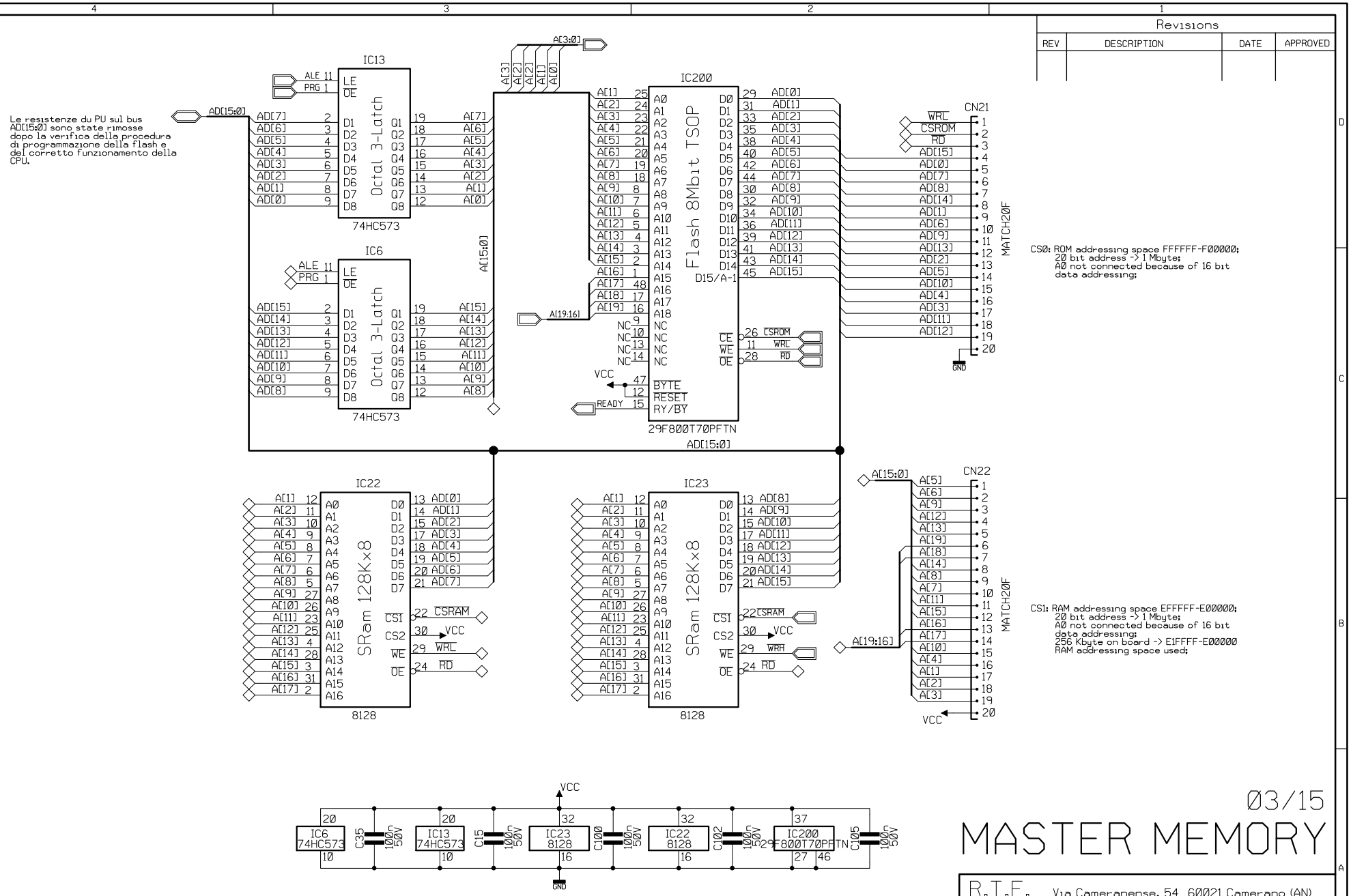
H=4ND; V=4LA



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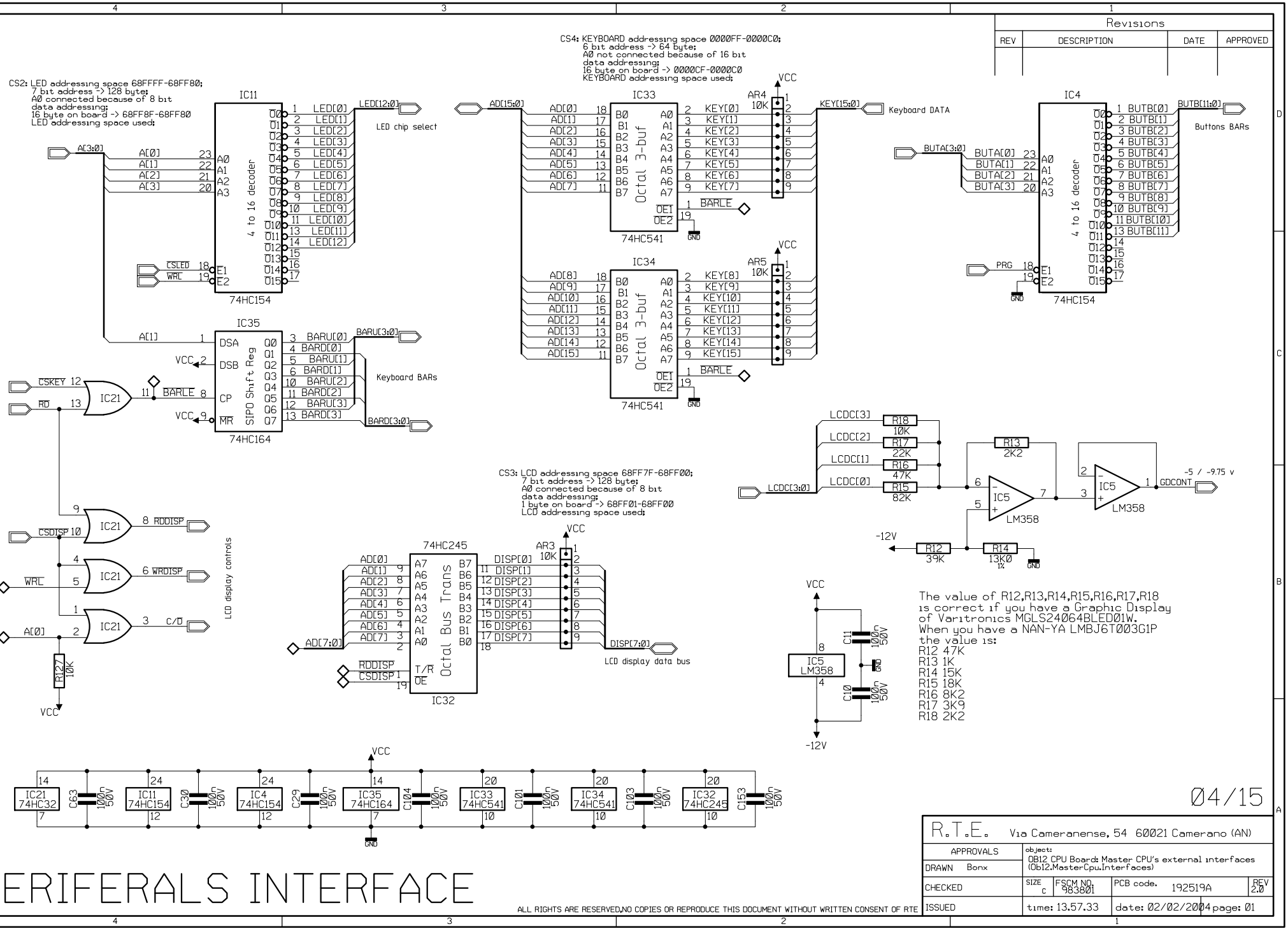
H=4ND; V=4LA


Revisions
REV
DESCRIPTION
DATE
APPROVED
CS2: LED addressing space 68FFFF-68FF80;
7 bit address -> 128 byte;
A0 connected because of 8 bit
data addressing;
16 byte on board -> 68FF8F-68FF80
LED addressing space used:
IC11
4 to 16 decoder
74HC154
LED[12:0]
LED chip select
CSLED
WRL
CS4: KEYBOARD addressing space 0000FF-0000C0;
6 bit address -> 64 byte;
A0 not connected because of 16 bit
data addressing;
16 byte on board -> 0000CF-0000C0
KEYBOARD addressing space used:
IC33
Octal 3-buf
74HC541
AR4
10K
KEY[15:0]
Keyboard DATA
IC34
AR5
10K
IC4
4 to 16 decoder
74HC154
BUTB[11:0]
Buttons BARs
PRG
IC35
SIPO Shift Reg
74HC164
BARU[3:0]
BARD[3:0]
Keyboard BARs
CSKEY
RD
IC21
BARLE
LCD display controls
RDDISP
CSDISP
WRL
C/D
R127
10K
CS3: LCD addressing space 68FF7F-68FF00;
7 bit address -> 128 byte;
A0 connected because of 8 bit
data addressing;
1 byte on board -> 68FF01-68FF00
LCD addressing space used:
74HC245
Octal Bus Trans
IC32
AR3
10K
DISP[7:0]
LCD display data bus
LCDC[3:0]
R18
10K
R17
22K
R16
47K
R15
82K
R13
2K2
IC5
LM358
GDCONT
-5 / -9.75 v
-12V
R12
39K
R14
13K0
1%
C11
C10
100n
50V
The value of R12,R13,R14,R15,R16,R17,R18
is correct if you have a Graphic Display
of Varitronics MGLS24064BLED01W.
When you have a NAN-YA LMBJ6T003G1P
the value is:
R12 47K
R13 1K
R14 15K
R15 18K
R16 8K2
R17 3K9
R18 2K2
IC21 74HC32
IC11 74HC154
IC4 74HC154
IC35 74HC164
IC33 74HC541
IC34 74HC541
IC32 74HC245
C63
C30
C29
C104
C101
C103
C153
GND
04/15
PERIFERALS INTERFACE
R.T.E. Via Cameranense, 54 60021 Camerano (AN)
APPROVALS
DRAWN Bonx
CHECKED
ISSUED
object:
OB12 CPU Board: Master CPU's external interfaces
(Ob12.MasterCpu.Interfaces)
SIZE C
FSCM NO 983801
PCB code. 192519A
REV 2.0
time: 13.57.33
date: 02/02/2004
page: 01
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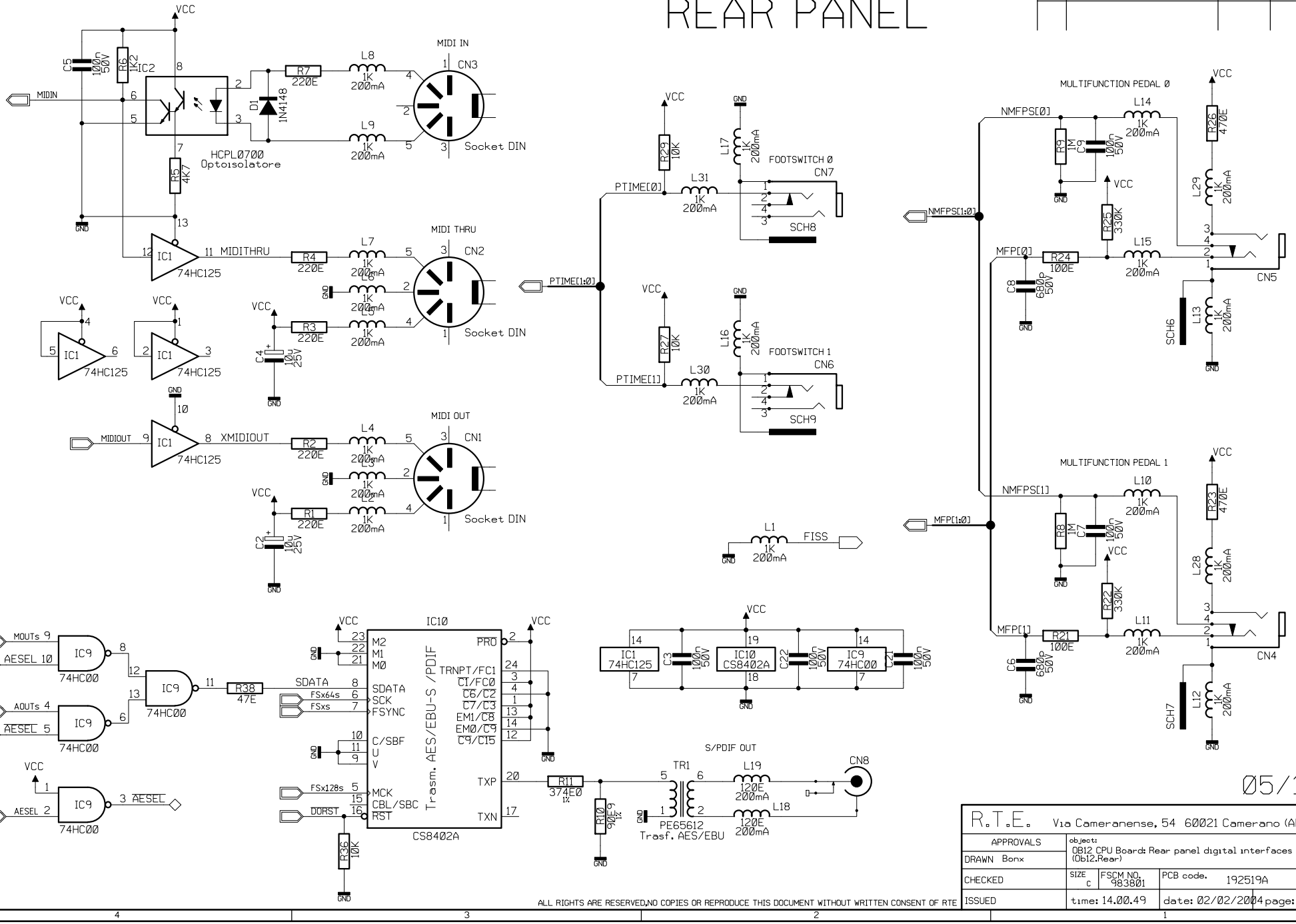
H=4ND; V=4LA

REAR PANEL

Revisions			
REV	DESCRIPTION	DATE	APPROVED



05/15

R.T.E.	Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Rear panel digital interfaces (Ob12.Rear)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A	REV 2.0
ISSUED	time: 14.00.49		date: 02/02/2004	page: 01

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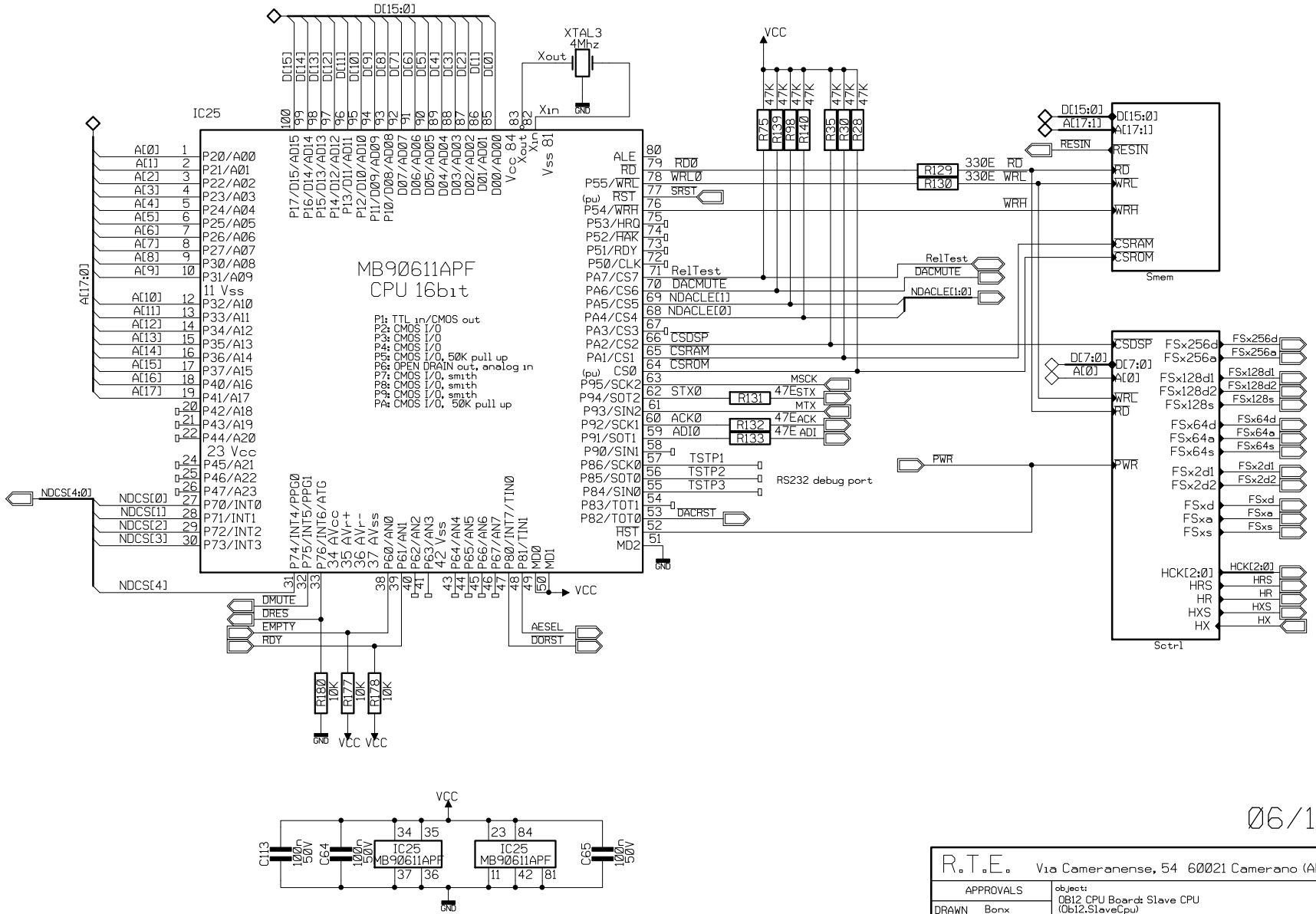
H=4ND; V=4LA

SLAVE CPU

Revisions			
REV	DESCRIPTION	DATE	APPROVED



R.T.E.	Via Cameranense, 54 60021 Camerano (AN)		
APPROVALS	object: OB12 CPU Board: Slave CPU (Ob12.SlaveCpu)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A REV 2.0
ISSUED	time: 14.04.37		date: 02/02/2004 page: 01

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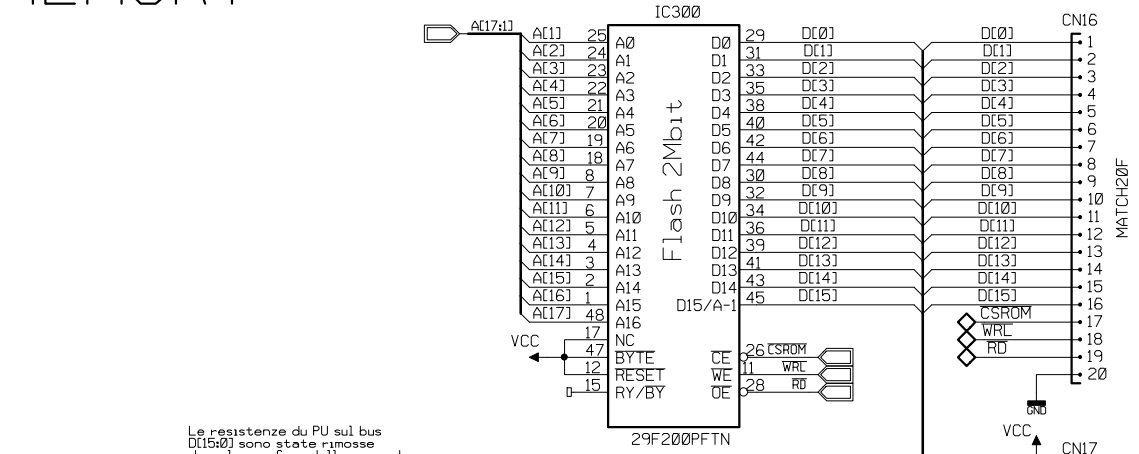
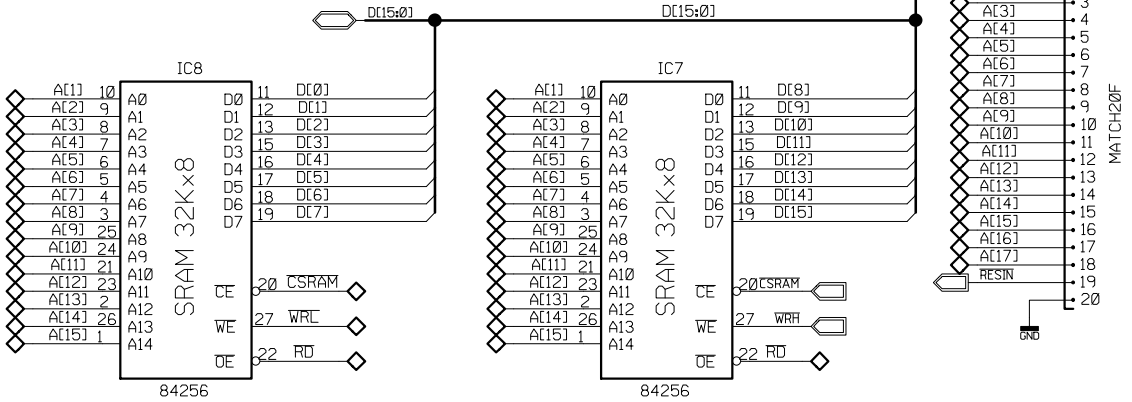
H=4ND; V=4LA

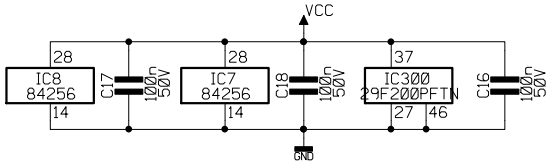
SLAVE MEMORY

Revisions			
REV	DESCRIPTION	DATE	APPROVED



Le resistenze du PU sul bus D[15:0] sono state rimosse dopo la verifica della procedura di programmazione della flash e del corretto funzionamento della CPU.





07/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Slave CPU's memory (Ob12.SlaveCpu.Smem)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A REV 2.0
ISSUED	time: 14.05.57	date: 02/02/2004	page: 01

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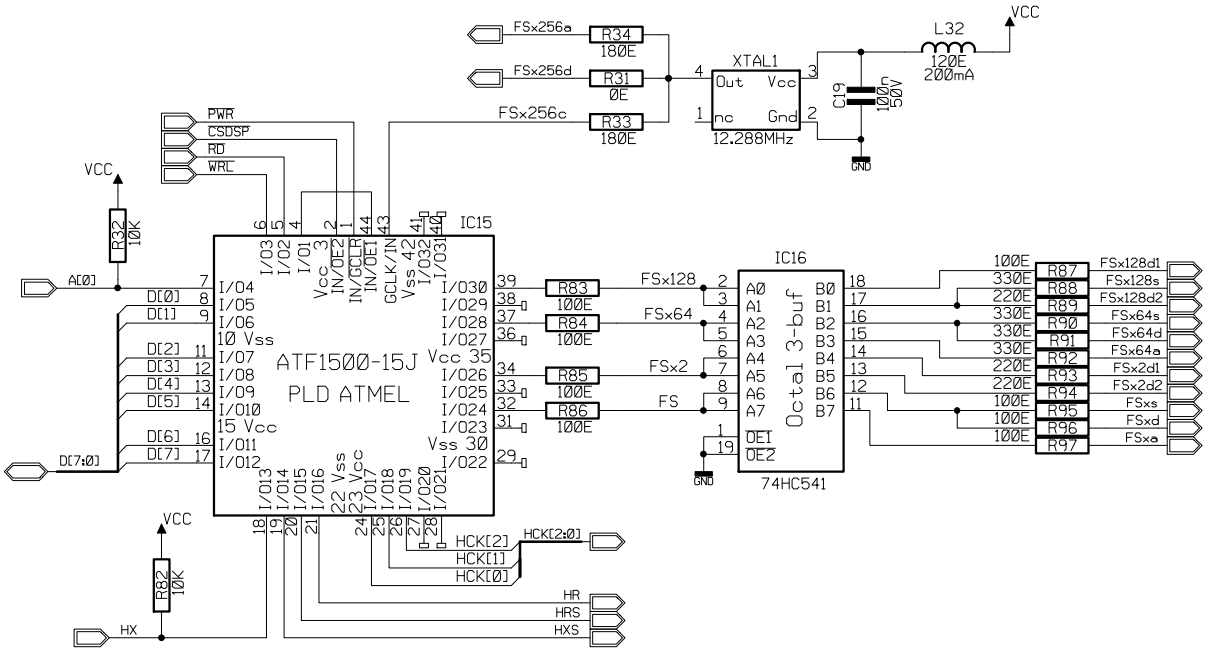
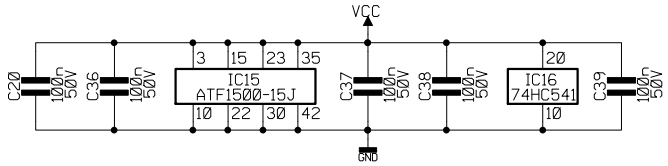
H=4ND; V=4LA

DASPs CONTROL

Revisions			
REV	DESCRIPTION	DATE	APPROVED





08/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)				
APPROVALS	object: OB12 CPU Board: Audio generator's Slave interface (Ob12.SlaveCpu.Sctrl)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A	REV 2.0
ISSUED	time: 14.07.13		date: 02/02/2004	page: 01

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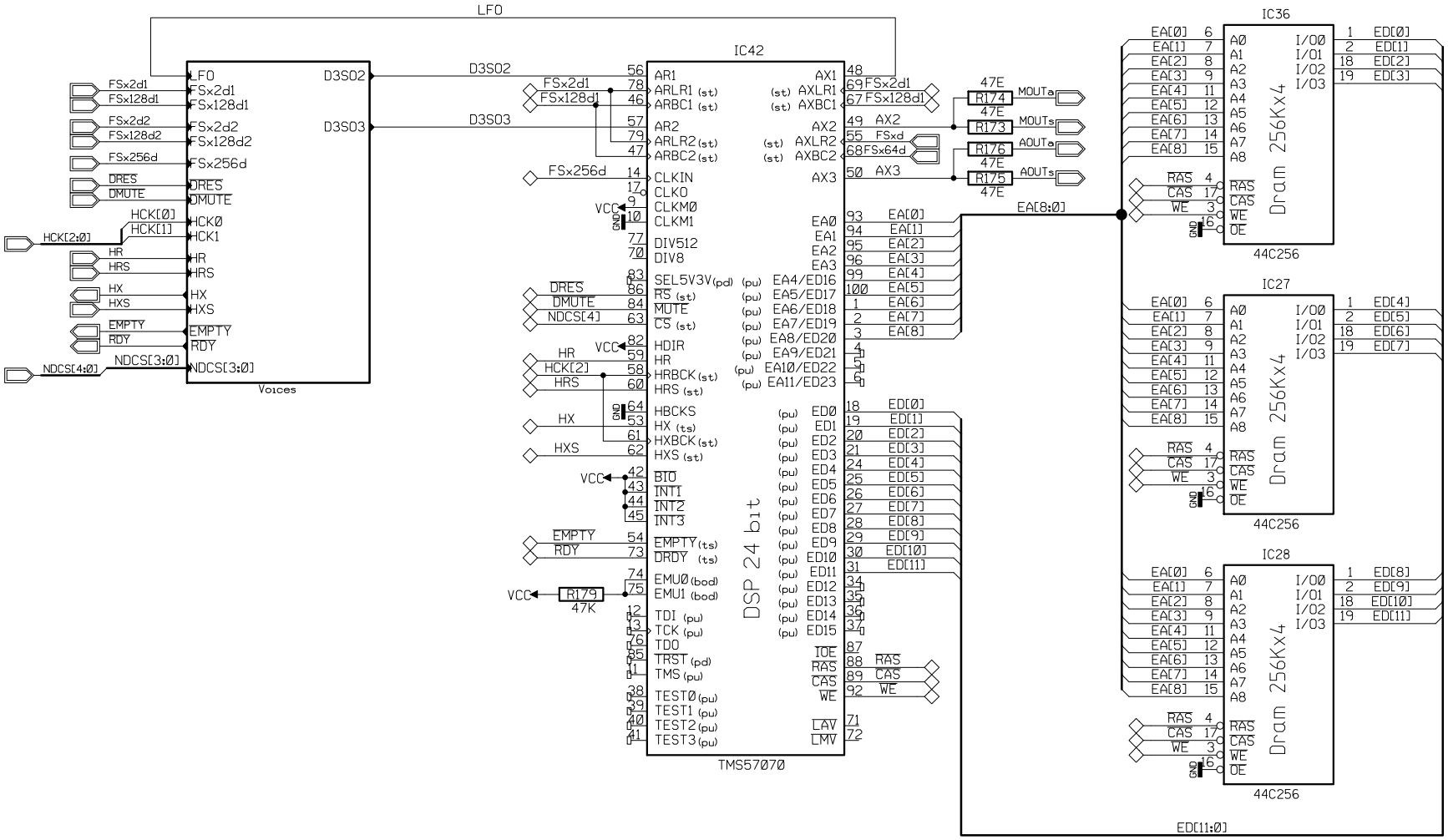
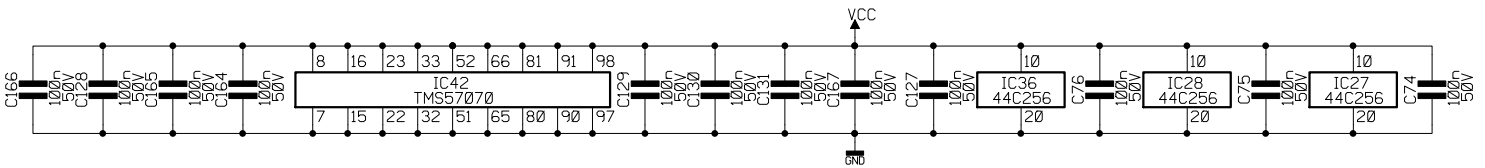
H=4ND; V=4LA

Revisions			
REV	DESCRIPTION	DATE	APPROVED

DASP[3:0] VOICEs GENERATOR

DASP[4] LFO & EFFECT GENERATOR





09/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)

APPROVALS	object: OB12 CPU Board: Audio generator (Ob12.Dasp)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A	REV 2.0
ISSUED	time: 14.09.01		date: 02/02/2004	page: 01

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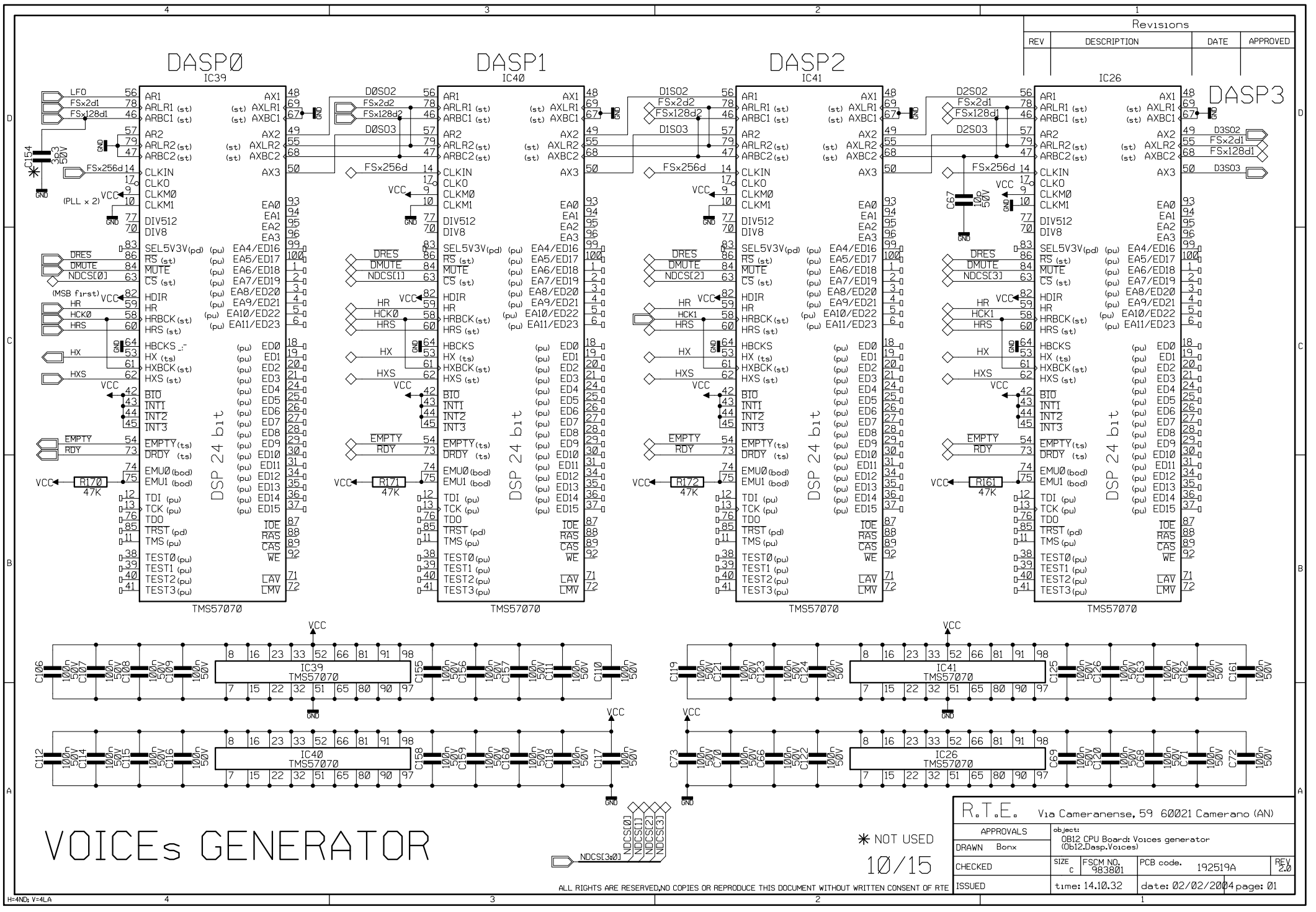
H=4ND; V=4LA


DASP0
IC39
DASP1
IC40
DASP2
IC41
IC26
DASP3
DSP 24 bit
TMS57070
VOICEs GENERATOR
R.T.E. Via Cameranense, 59 60021 Camerano (AN)
NOT USED
10/15
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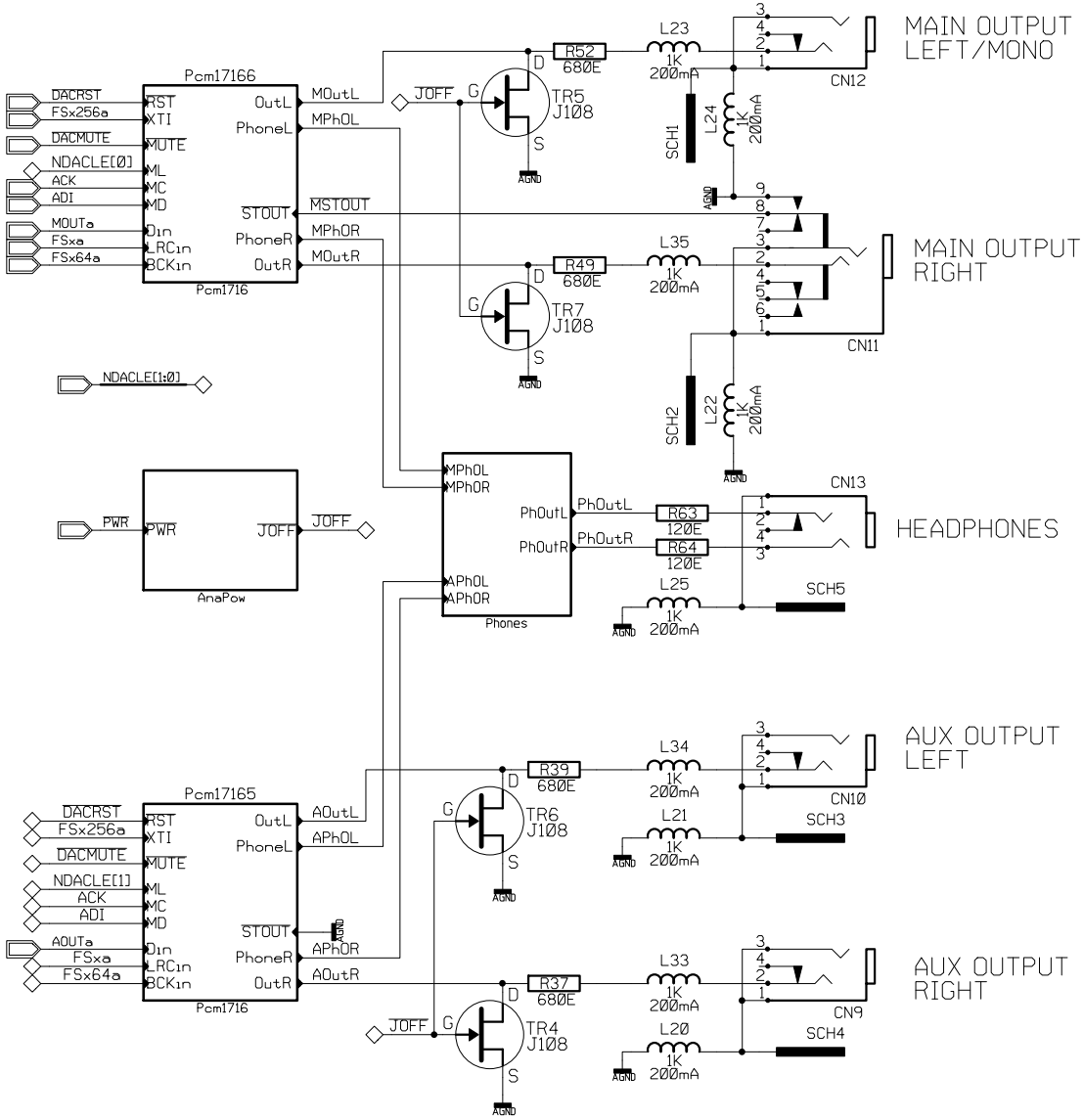
ANALOG OUTPUTs

Revisions			
REV	DESCRIPTION	DATE	APPROVED



11/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: Analog circuits (Ob12.Analog)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A / REV 2.0
ISSUED	time: 14.20.53	date: 02/02/2004	page: 01

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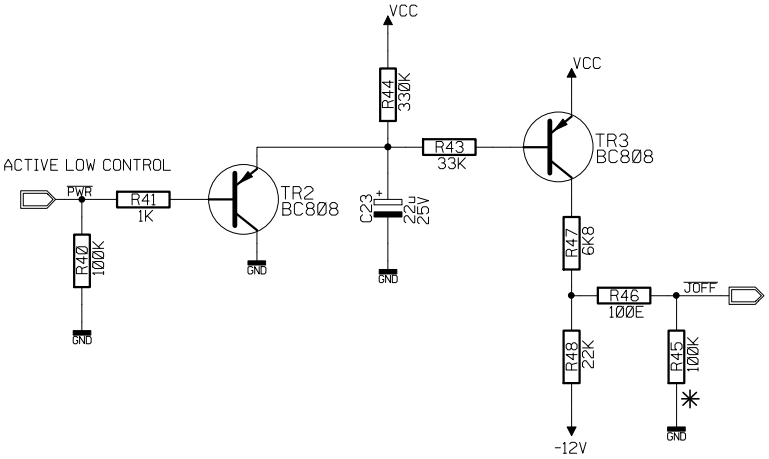
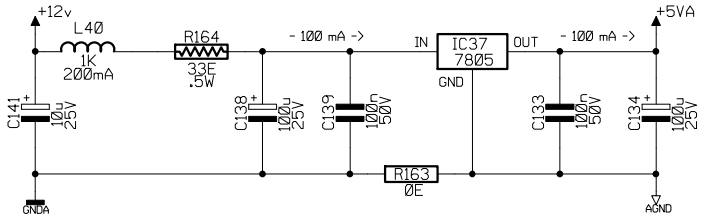
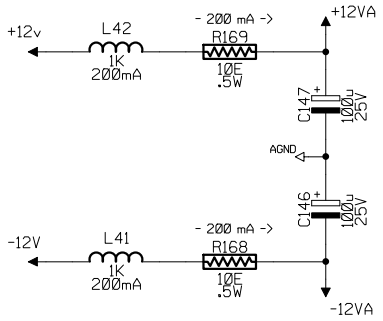
H=4ND; V=4LA

ANALOG POWER SUPPLY

Revisions			
REV	DESCRIPTION	DATE	APPROVED







12/15

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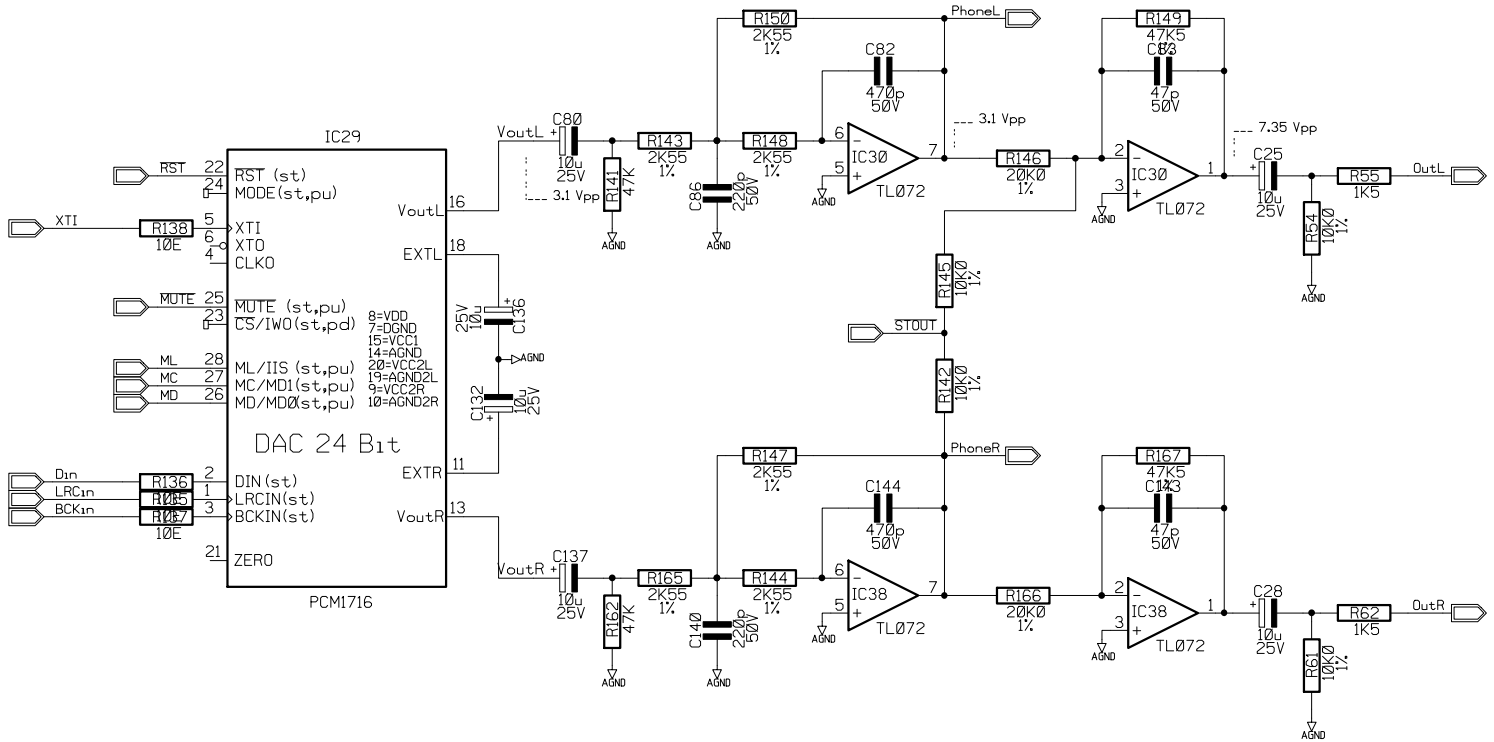
R.T.E. Via Cameranense, 54 60021 Camerano (AN)				
APPROVALS	object: OB12 CPU Board: Analog circuit's power supply (Ob12.Analog.AnaPow)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A	REV 2.0
ISSUED	time: 14.20.38		date: 02/02/2004	page: 01

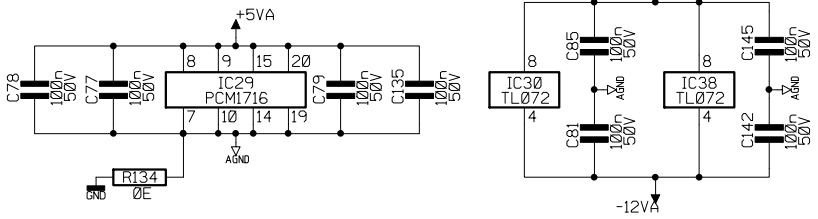
H=4ND; V=4LA

OUTPUT STEREO CHANNEL

Revisions			
REV	DESCRIPTION	DATE	APPROVED

Ft1 = 47.0 KHz; G = 1;
Ft2 = 70.5 KHz; G = 2.37;
Ft = 36.0 KHz; G = 2.37 (7.5 dB);





13-14/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)				
APPROVALS	object: OB12 CPU Board: D to A conversion stereo channel (Ob12.Analog.Pcm1716)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A	REV 2.0
ISSUED	time: 14.23.36		date: 02/02/2004	page: 01

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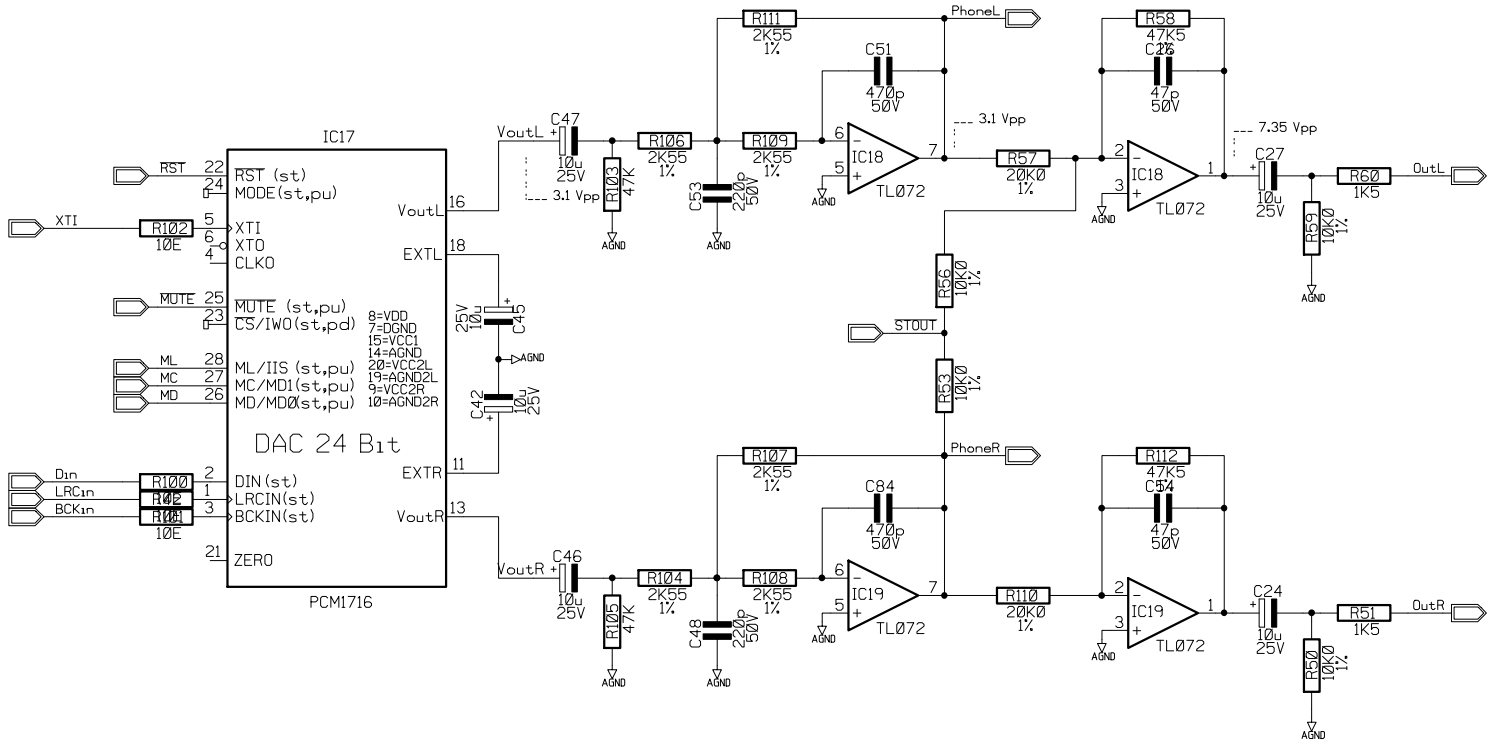
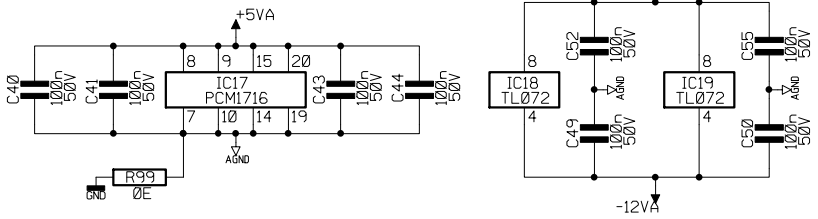
H=4ND; V=4LA

OUTPUT STEREO CHANNEL

Revisions			
REV	DESCRIPTION	DATE	APPROVED

Ft1 = 47.0 KHz; G = 1;
Ft2 = 70.5 KHz; G = 2.37;
Ft = 36.0 KHz; G = 2.37 (7.5 dB);





13-14/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)				
APPROVALS	object: OB12 CPU Board: D to A conversion stereo channel (Ob12.Analog.Pcm1716)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO. 983801	PCB code. 192519A	REV 2.0
ISSUED	time: 14.23.36		date: 02/02/2004	page: 01

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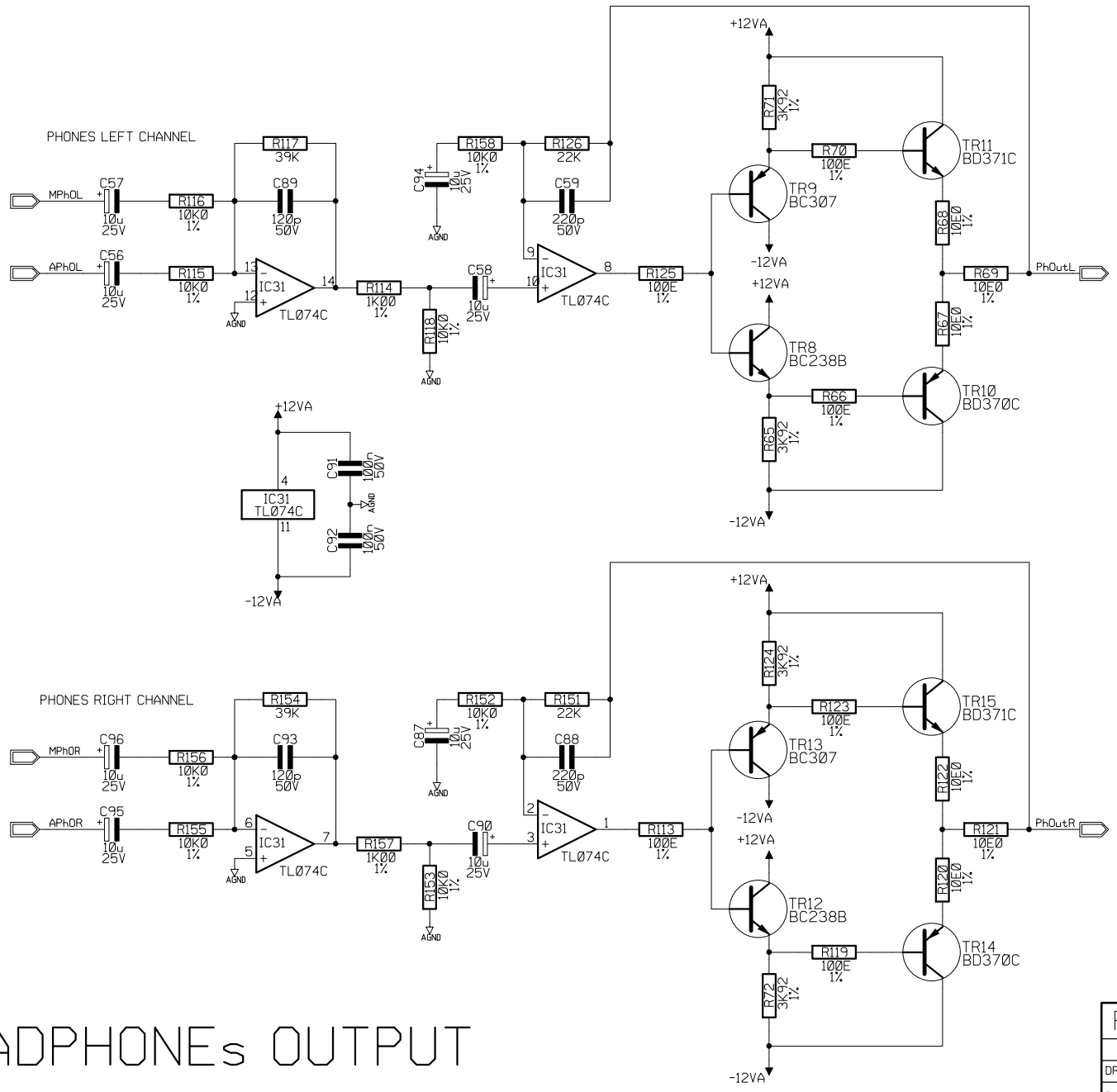
H=4ND; V=4LA



HEADPHONEs OUTPUT

Revisions			
REV	DESCRIPTION	DATE	APPROVED

15/15

R.T.E. Via Cameranense, 54 60021 Camerano (AN)			
APPROVALS	object: OB12 CPU Board: HeadPhones Output (Ob12.Analog.Phones)		
DRAWN Bonx			
CHECKED	SIZE C / FSCM NO. 983801	PCB code. 192519A	REV 2.0
ISSUED	time: 14.28.10	date: 02/02/2004	page: 01

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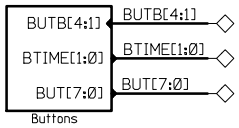
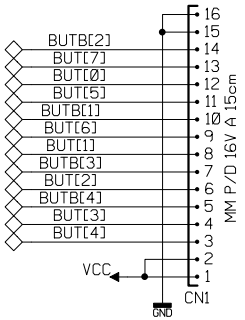
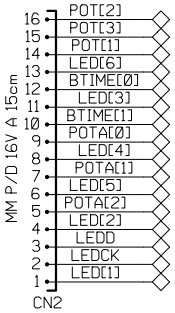
H=4ND; V=4LA

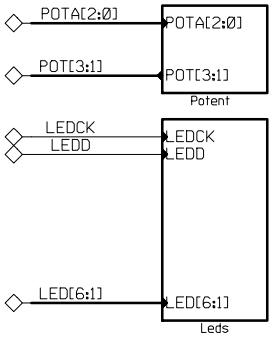
PANEL A CONNECTOR

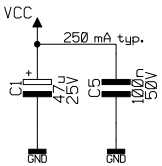
Revisions			
REV	DESCRIPTION	DATE	APPROVED











R.T.E. Via Cameranense, 59 60021 Camerano (AN)				
APPROVALS	object: OB12 Panel A: Top Level (Panel A)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO.	PCB code. 192521	REV 1.0
ISSUED	time: 17.30.11		date: 2000.03.08	page: 01

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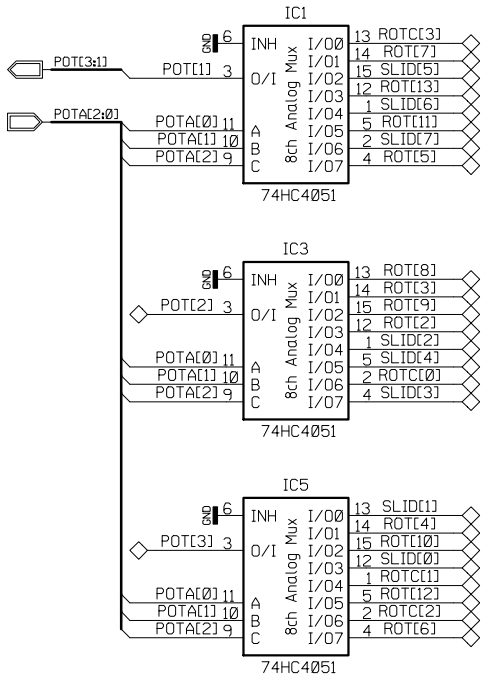

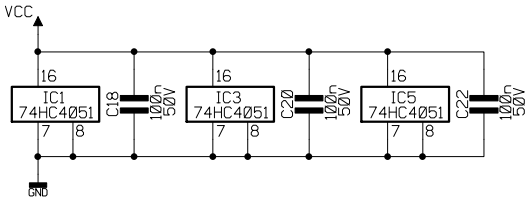

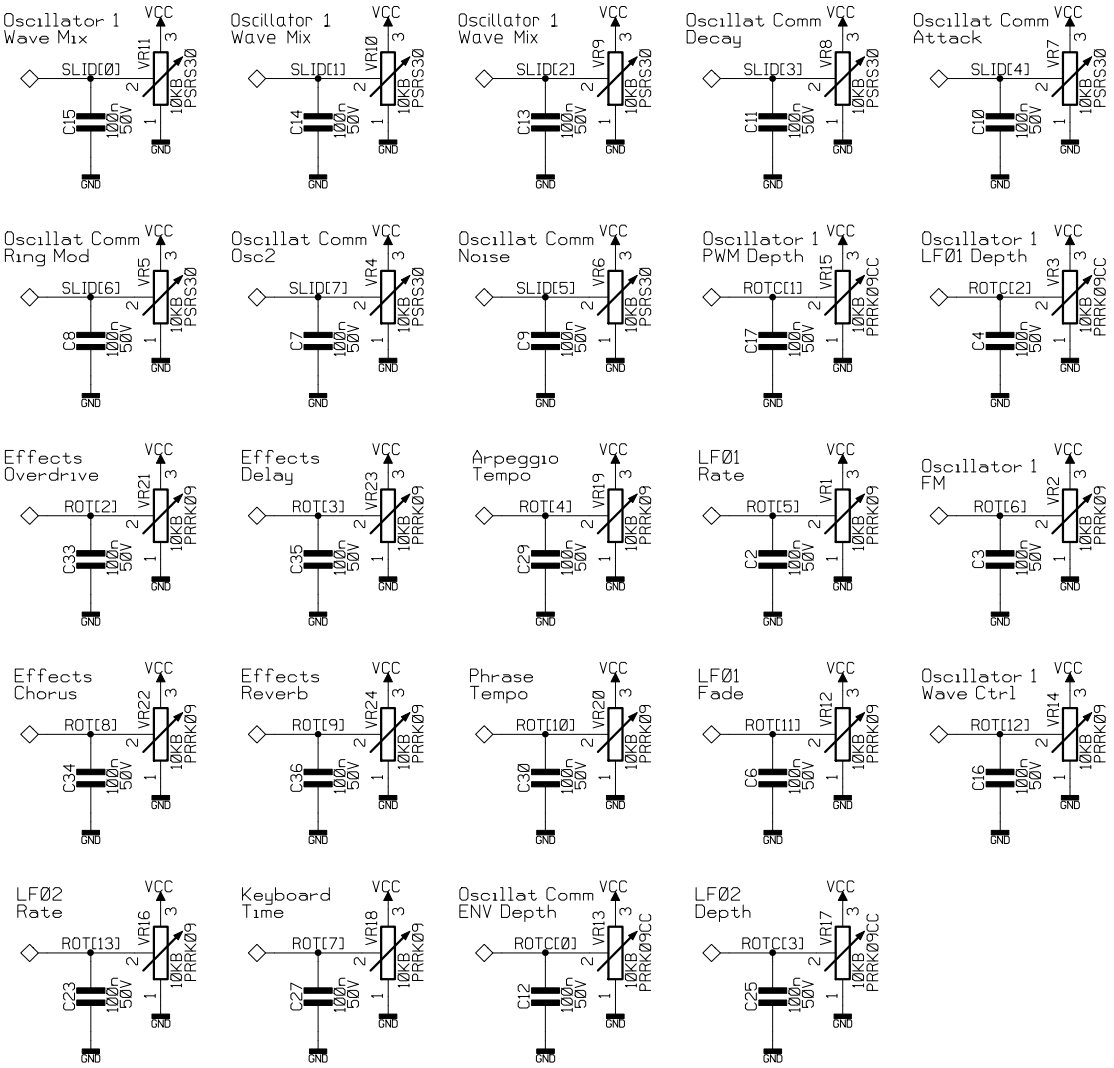

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4 VR2 POTRKØ9_1ØKB_ALPS
4 VR3 POTRKØ9_1ØKBCC_ALPS
4 VR4 POTRS3ØM1ØKB
4 VR5 POTRS3ØM1ØKB
4 VR6 POTRS3ØM1ØKB
4 VR7 POTRS3ØM1ØKB
4 VR8 POTRS3ØM1ØKB
4 VR9 POTRS3ØM1ØKB
4 VR1Ø POTRS3ØM1ØKB
4 VR11 POTRS3ØM1ØKB
4 VR12 POTRKØ9_1ØKB_ALPS
4 VR13 POTRKØ9_1ØKBCC_ALPS
4 VR14 POTRKØ9_1ØKB_ALPS
4 VR15 POTRKØ9_1ØKBCC_ALPS
4 VR16 POTRKØ9_1ØKB_ALPS
4 VR17 POTRKØ9_1ØKBCC_ALPS
4 VR18 POTRKØ9_1ØKB_ALPS
4 VR19 POTRKØ9_1ØKB_ALPS
4 VR2Ø POTRKØ9_1ØKB_ALPS
4 VR21 POTRKØ9_1ØKB_ALPS
4 VR22 POTRKØ9_1ØKB_ALPS
4 VR23 POTRKØ9_1ØKB_ALPS
4 VR24 POTRKØ9_1ØKB_ALPS
GND

R.T.E. Via Cameranense, 59 60021 Camerano (AN)			
APPROVALS	object: OB12 Panel A: Potentiometers (Panel A.Potent)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. 192521 REV 1.Ø
ISSUED	time: Ø9.11.38		date: 2000.03.09 page: Ø1

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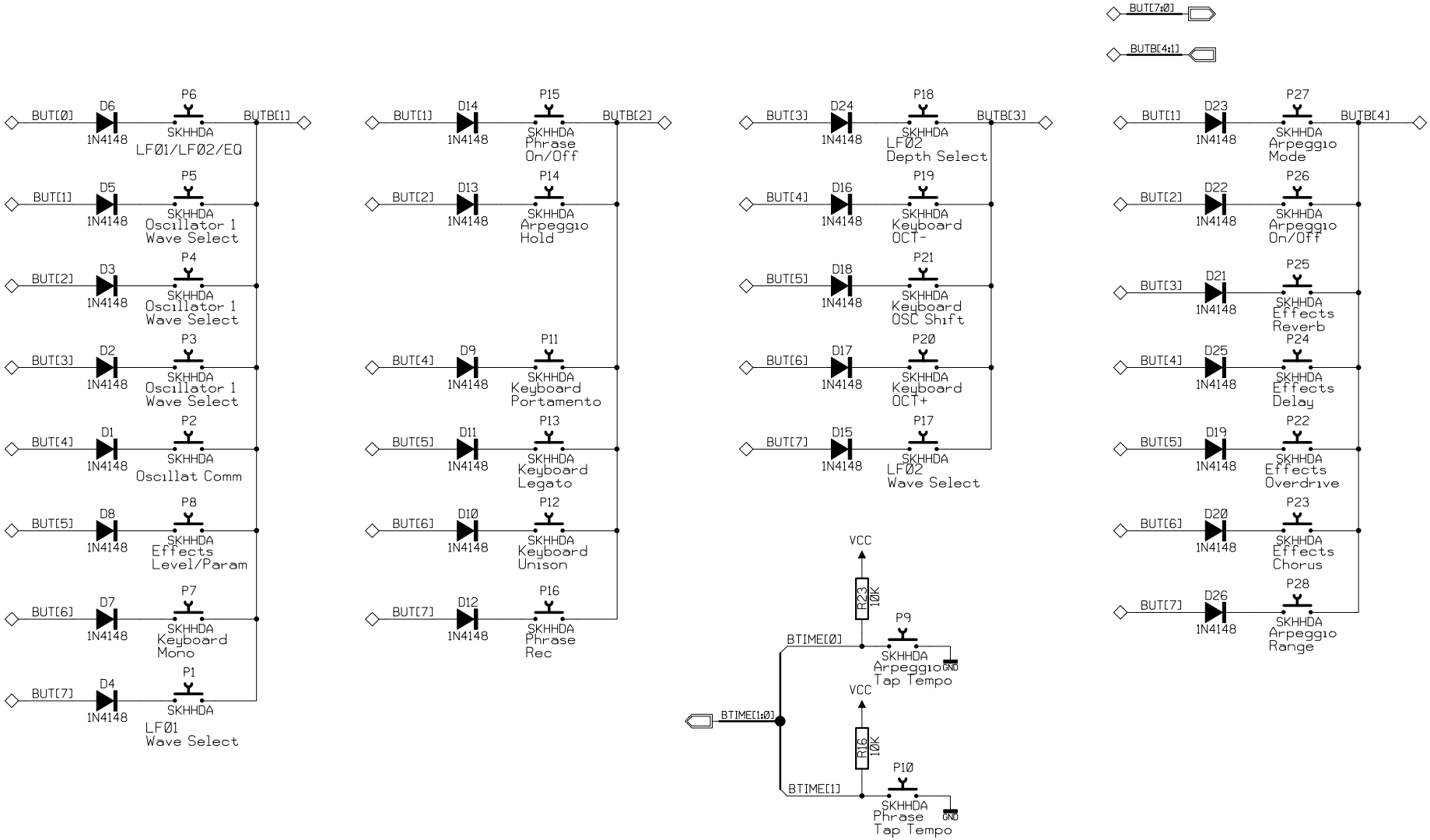

R.T.E.	Via Cameranense, 59 60021 Camerano (AN)			
APPROVALS	object: OB12 Panel A: Buttons (Panel A.Buttons)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO.	PCB code. 192521	REV 1.0
ISSUED	time: 10.44.22		date: 2000.03.09	page: 01

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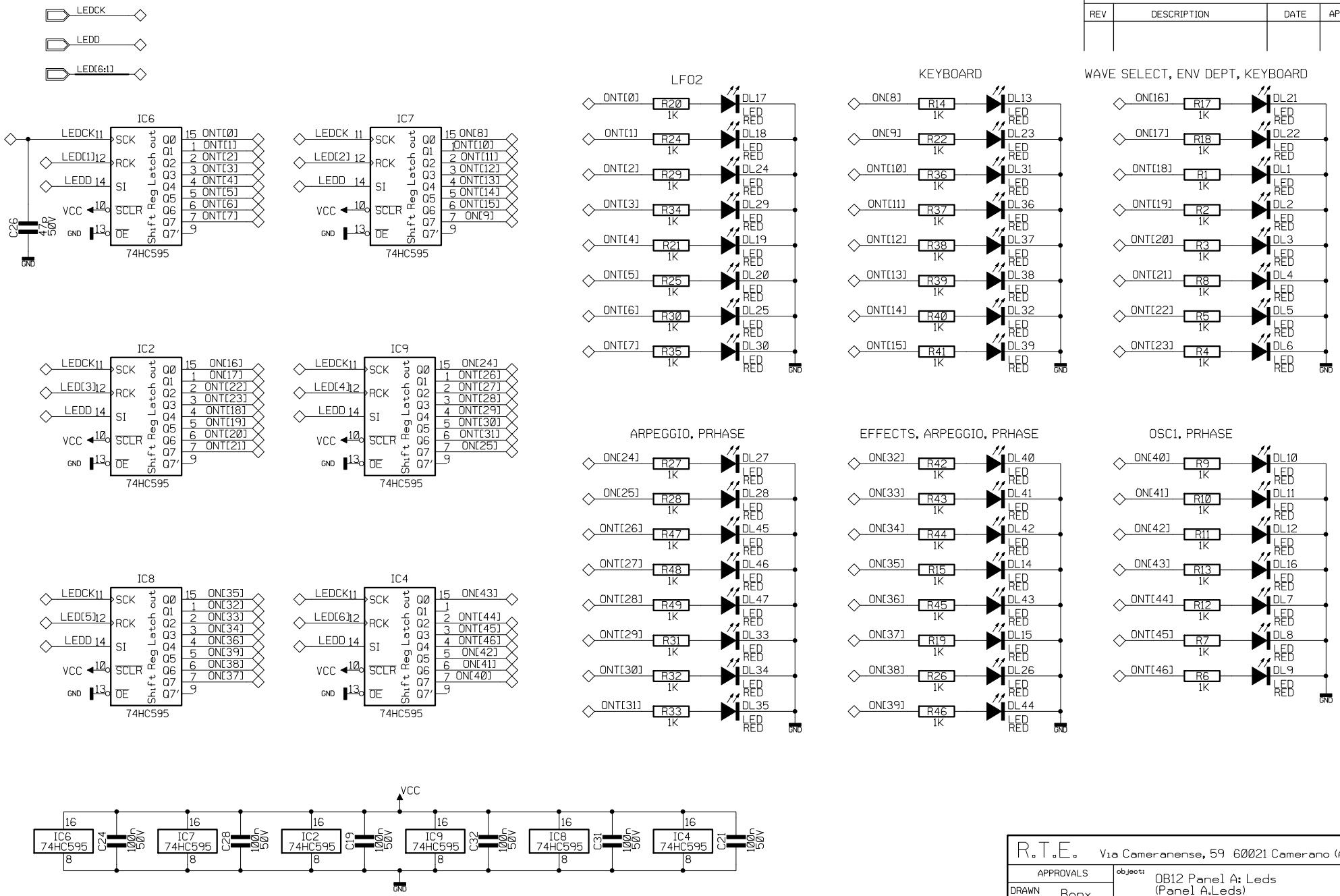

Revisions

REV	DESCRIPTION	DATE	APPROVED

R.T.E. Via Cameranense, 59 60021 Camerano (AN)			
APPROVALS	object: OB12 Panel A: Leds (Panel A.Leds)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. 192521 REV 1.0
ISSUED	time: 10.46.28	date: 2000.03.09	page: 01

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PANEL B CONNECTOR

Revisions			
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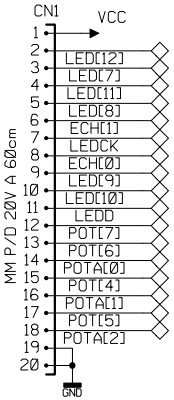

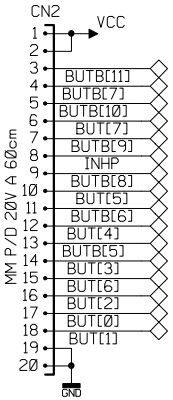

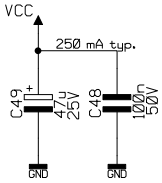

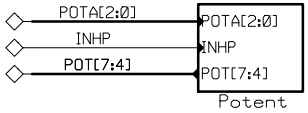

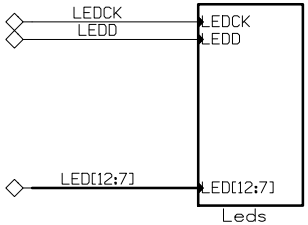

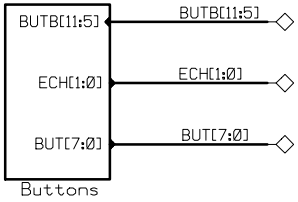

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R.T.E. Via Cameranense, 59 60021 Camerano (AN)				
APPROVALS	object: OB12 Panel B: Top Level (Panel B)			
DRAWN Bonx				
CHECKED	SIZE C	FSCM NO.	PCB code. 192522	REV 1.0
ISSUED	time: 17.05.43		date: 2000.03.08	page: 01

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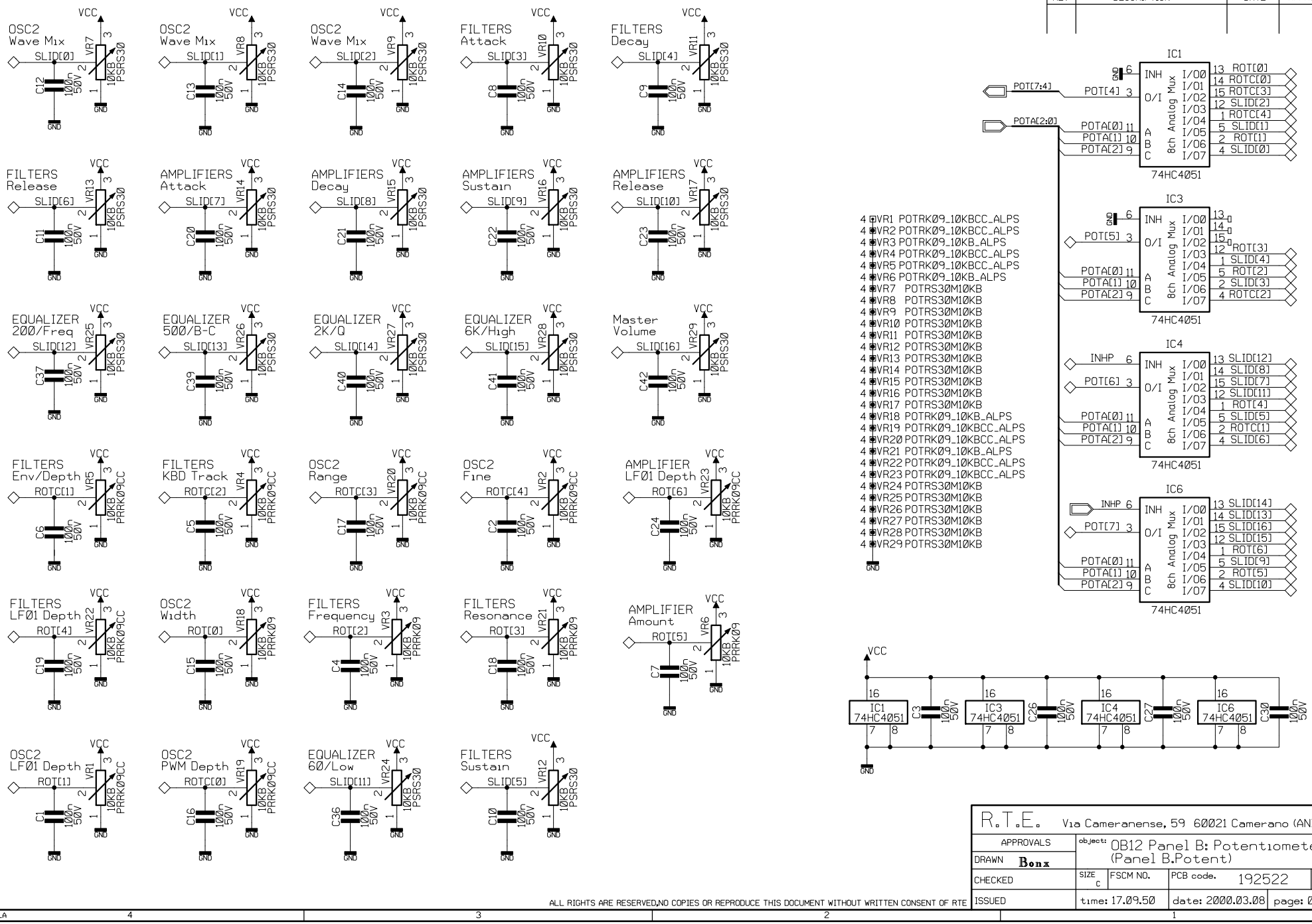

Revisions

REV	DESCRIPTION	DATE	APPROVED

R.T.E. Via Cameranense, 59 60021 Camerano (AN)			
APPROVALS	object: OB12 Panel B: Potentiometers (Panel B.Potent)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. 192522 REV 1.0
ISSUED	time: 17.09.50	date: 2000.03.08	page: Ø1

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Revisions			
REV	DESCRIPTION	DATE	APPROVED

Filters FILTER 1

BUT[0]	D8 1N4148	P8 SKHHDA	BUTB[5]
BUT[1]	D7 1N4148	P7 SKHHDA	Oscillator 2 KBD TRACK
BUT[2]	D6 1N4148	P6 SKHHDA	Oscillator 2 LF01/LF02/EQ
BUT[3]	D5 1N4148	P5 SKHHDA	Oscillator 2 WAVE SELECT
BUT[4]	D4 1N4148	P4 SKHHDA	Oscillator 2 WAVE SELECT
BUT[5]	D3 1N4148	P3 SKHHDA	Oscillator 2 WAVE SELECT
BUT[6]	D9 1N4148	P9 SKHHDA	Filters FILTER 2
BUT[7]	D1 1N4148	P1 SKHHDA	Oscillator 2 SYNC

Cursor P12 8 VWX

BUT[0]	D12 1N4148	P12 SKHHDA	BUTB[6]
BUT[1]	D15 1N4148	P15 SKHHDA	Cursor 5 MNO
BUT[2]	D18 1N4148	P18 SKHHDA	Cursor 2 DEF
BUT[3]	D21 1N4148	P28 SKHHDA	Cursor SPACE
BUT[4]	D42 1N4148	P40 SKHHDA	Morph MANUAL
BUT[5]	D52 1N4148	P50 SKHHDA	Motion LOC 1
BUT[6]	D2 1N4148	P2 SKHHDA	Filters ROUTING
BUT[7]	D10 1N4148	P10 SKHHDA	Amplifier AUTOPAN

Cursor P13 9 YZ

BUT[0]	D13 1N4148	P13 SKHHDA	BUTB[7]
BUT[1]	D16 1N4148	P16 SKHHDA	Cursor 6 PQR
BUT[2]	D19 1N4148	P19 SKHHDA	Cursor 3 GHI
BUT[3]	D22 1N4148	P29 SKHHDA	Cursor ENTER
BUT[4]	D39 1N4148	P41 SKHHDA	Morph ENABLE
BUT[5]	D53 1N4148	P51 SKHHDA	Motion LOC 1
BUT[6]	D43 1N4148	P52 SKHHDA	Equalizer MID MODE
BUT[7]	D44 1N4148	P53 SKHHDA	Equalizer BY PASS

Cursor P11 7 STU

BUT[0]	D11 1N4148	P11 SKHHDA	BUTB[8]
BUT[1]	D14 1N4148	P14 SKHHDA	Cursor 4 JKL
BUT[2]	D17 1N4148	P17 SKHHDA	Cursor 1 ABC
BUT[3]	D20 1N4148	P27 SKHHDA	Cursor BANK
BUT[4]	D38 1N4148	P39 SKHHDA	Morph AUTO
BUT[5]	D41 1N4148	P49 SKHHDA	Motion LOC 1

Cursor ESC P20

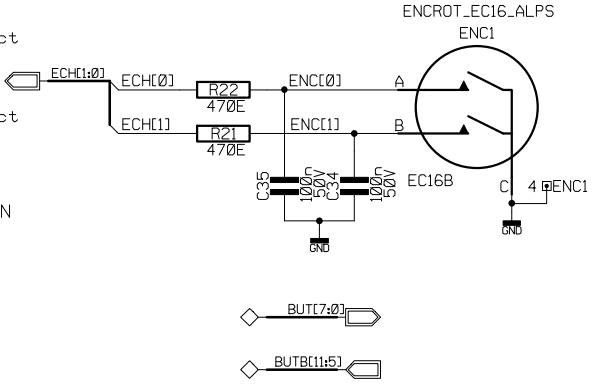
BUT[0]	D23 1N4148	P20 SKHHDA	BUTB[9]
BUT[1]	D24 1N4148	P21 SKHHDA	Cursor F1
BUT[2]	D25 1N4148	P22 SKHHDA	Cursor F2
BUT[3]	D26 1N4148	P23 SKHHDA	Cursor F3
BUT[4]	D27 1N4148	P24 SKHHDA	Cursor F4
BUT[5]	D35 1N4148	P25 SKHHDA	Cursor DISP HOLD
BUT[6]	D36 1N4148	P30 SKHHDA	Cursor LEFT
BUT[7]	D28 1N4148	P26 SKHHDA	Cursor UP

Keyb Mode P32 SPLIT

BUT[0]	D29 1N4148	P32 SKHHDA	BUTB[10]
BUT[1]	D30 1N4148	P33 SKHHDA	Keyb Mode LAYER
BUT[2]	D31 1N4148	P34 SKHHDA	Keyb Mode SINGLE
BUT[3]	D32 1N4148	P35 SKHHDA	Mode PROGRAM
BUT[4]	D33 1N4148	P36 SKHHDA	Mode TIMBRE
BUT[5]	D34 1N4148	P37 SKHHDA	Mode SYSTEM
BUT[6]	D40 1N4148	P38 SKHHDA	Cursor DOWN
BUT[7]	D37 1N4148	P31 SKHHDA	Cursor RIGHT

Part Select PART 1 P42

BUT[0]	D46 1N4148	P42 SKHHDA	BUTB[11]
BUT[1]	D45 1N4148	P43 SKHHDA	Part Select PART 2
BUT[2]	D47 1N4148	P44 SKHHDA	Part Select PART 3
BUT[3]	D49 1N4148	P46 SKHHDA	Set-Up PANEL SCAN
BUT[4]	D50 1N4148	P47 SKHHDA	Set-Up ROUTERS
BUT[5]	D51 1N4148	P48 SKHHDA	Set-Up WRITE
BUT[6]	D48 1N4148	P45 SKHHDA	Part Select PART 4



R.T.E.	Via Cameranense, 59 60021 Camerano (AN)		
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DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. 192522 REV 1.0
ISSUED	time: 14.36.41		date: 2000.03.09 page: 01

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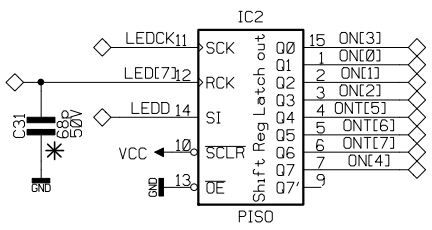
LEDCK

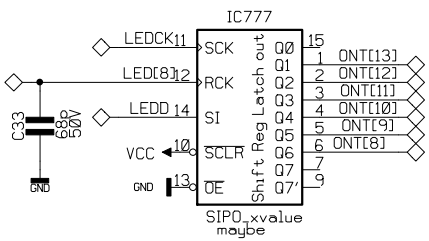
LEDD

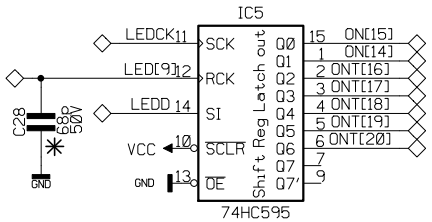
LED[12:7]

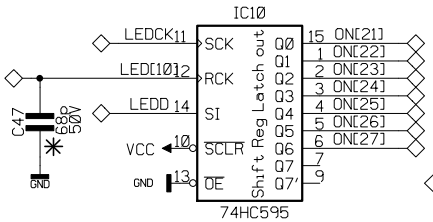
Revisions

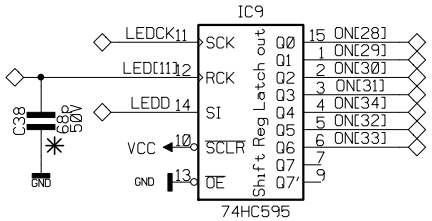
REV	DESCRIPTION	DATE	APPROVED

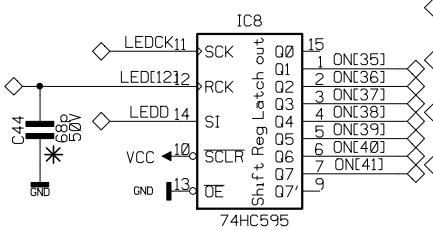


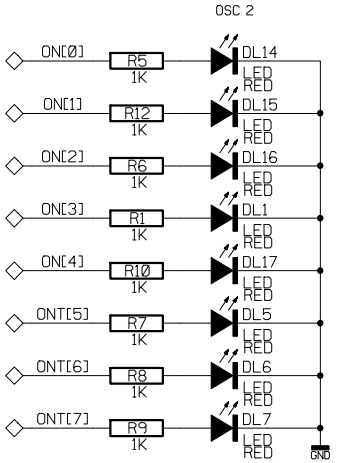


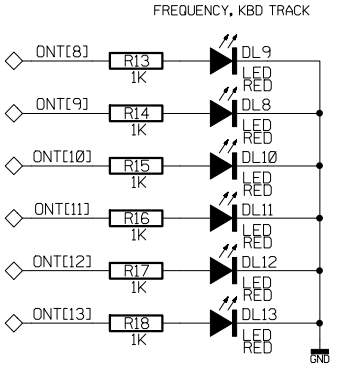


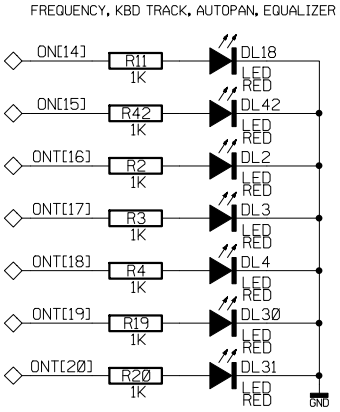


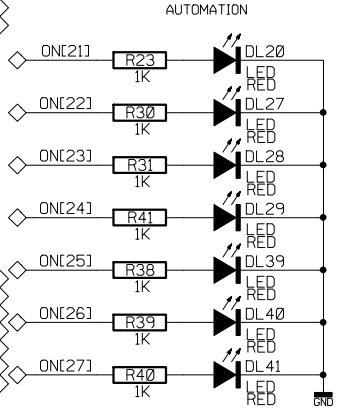


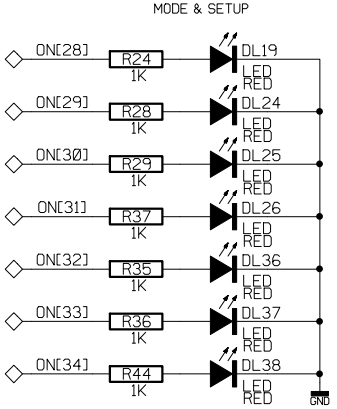


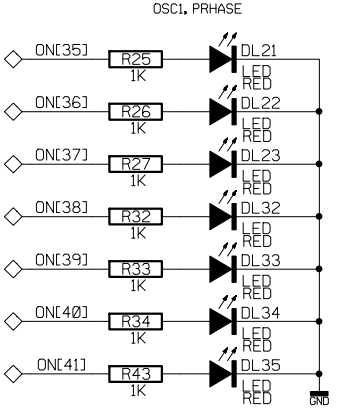


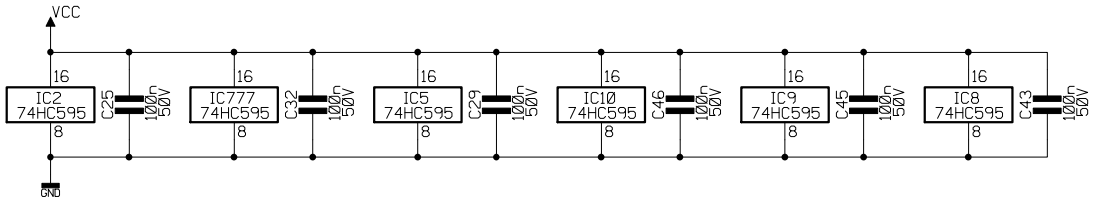












✳ NOT USED

R.T.E. Via Cameranense, 59 60021 Camerano (AN)			
APPROVALS	object: OB12 Panel B: Leds (Panel B.Leds)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. 192522 REV 1.0
ISSUED	time: 17.07.55	date: 2001.04.03	page: 01

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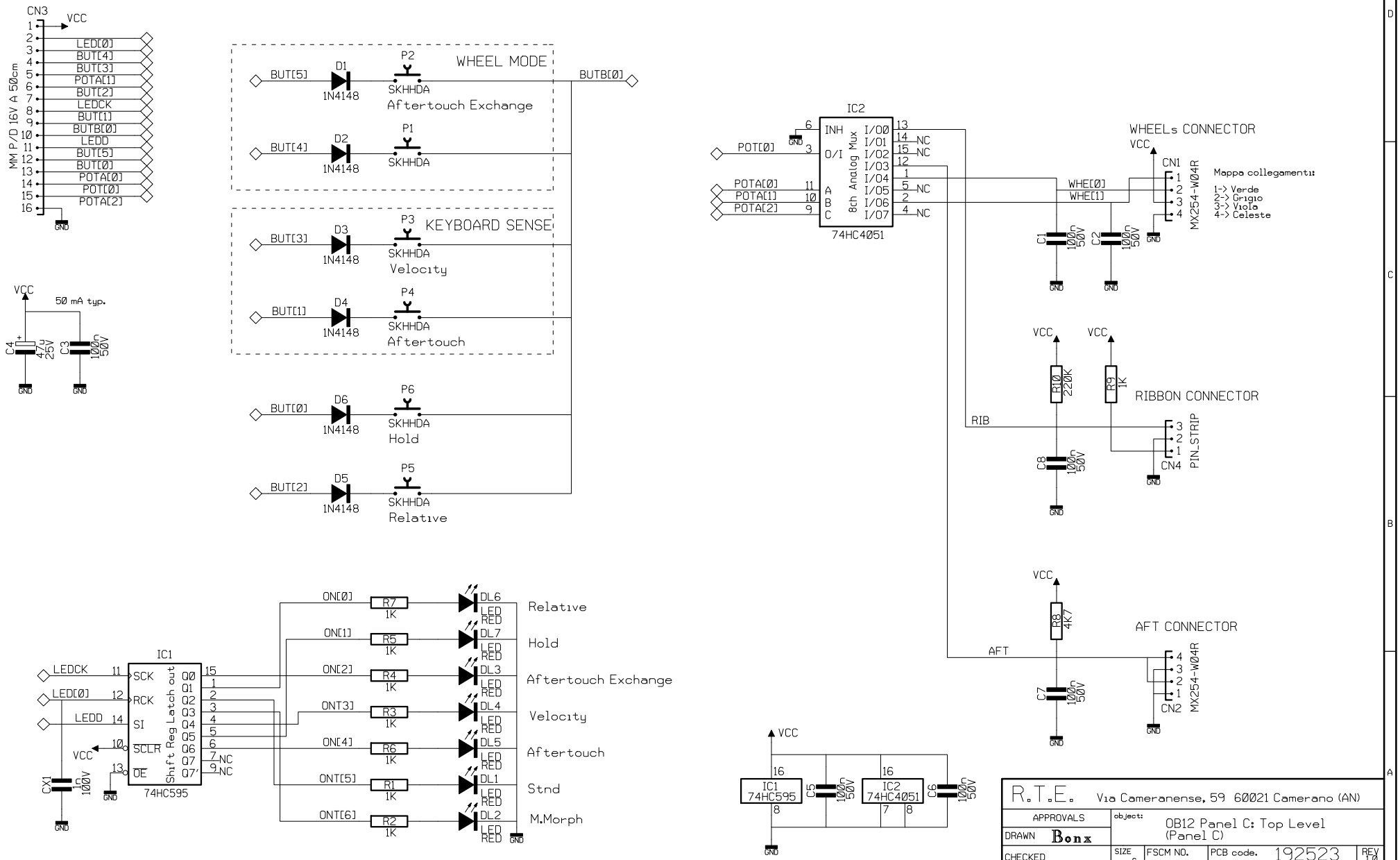
PANEL C CONNECTOR

Revisions			
REV	DESCRIPTION	DATE	APPROVED



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R.T.E. Via Cameranense, 59 60021 Camerano (AN)			
APPROVALS	object: OB12 Panel C: Top Level (Panel C)		
DRAWN Bonx			
CHECKED	SIZE C	FSCM NO.	PCB code. 192523 REV 1.0
ISSUED	time: 15.28.09	date: 2000.07.04	page: 01

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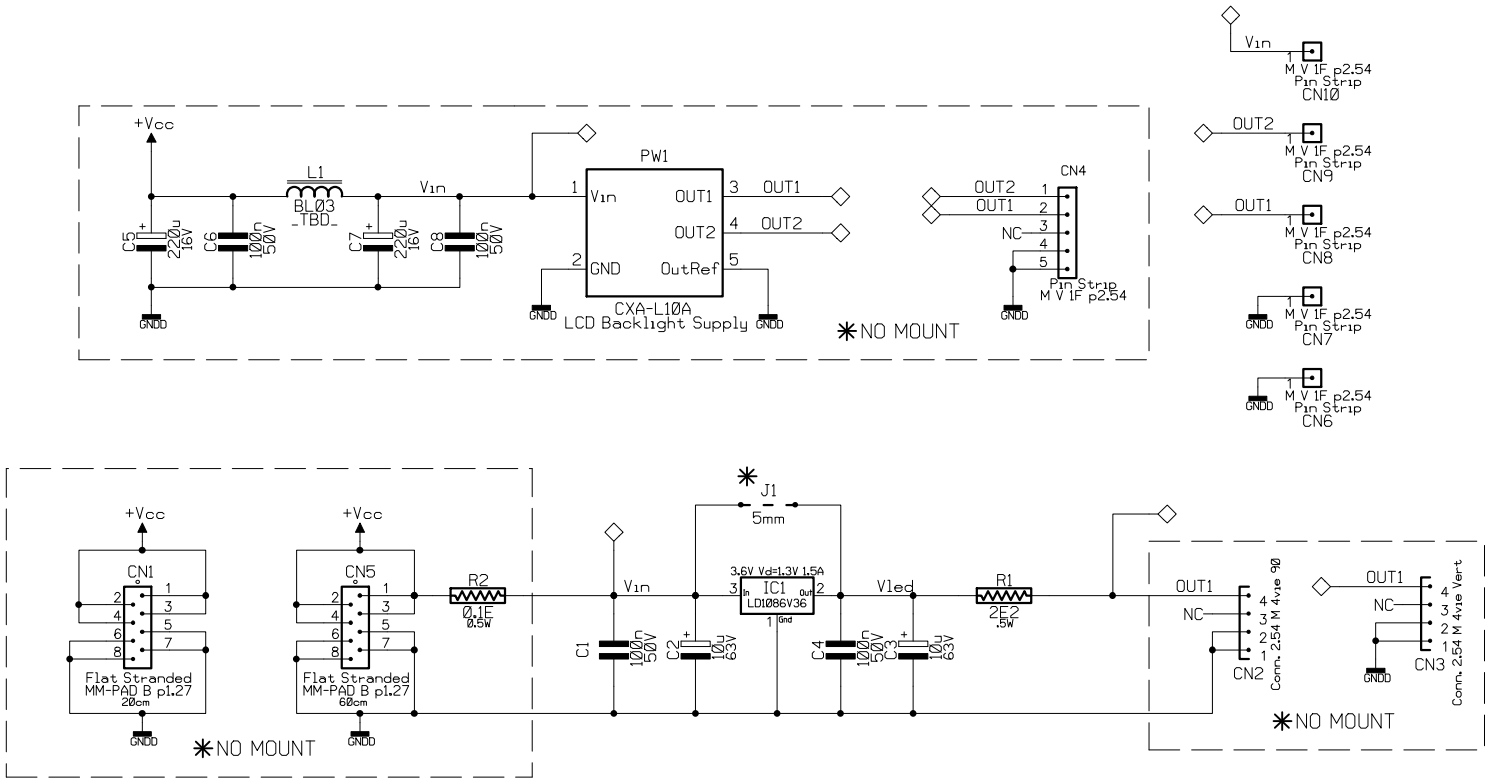

REV.	CMP. ref.	ZONE (Page/coords)	DESCRIPTION	DATE	Sign.

CONSORZIO R.T.E.
Via dell'Artigianato, 54
47835 Saludecio (RN) - ITALY
Tel.: +39-541-981709 Fax: +39-541-850052
e-mail: rte@hi-net.it

SCHEMATIC DIAGRAM:

POWER SUPPLAY LCD

PRODUCT NAME:

OB-12

DATE: 05/03/2004	REV.:		
DRW: B.M.	SCM: 192298A	VER.:	
CKD: B.ZATTINI	ASSY.: 983607	SIZE:	SCALE:
APP: B.ZATTINI	PCB: 192298A	DSK.:	Scm. page: 01

Notes: NO MOUNT

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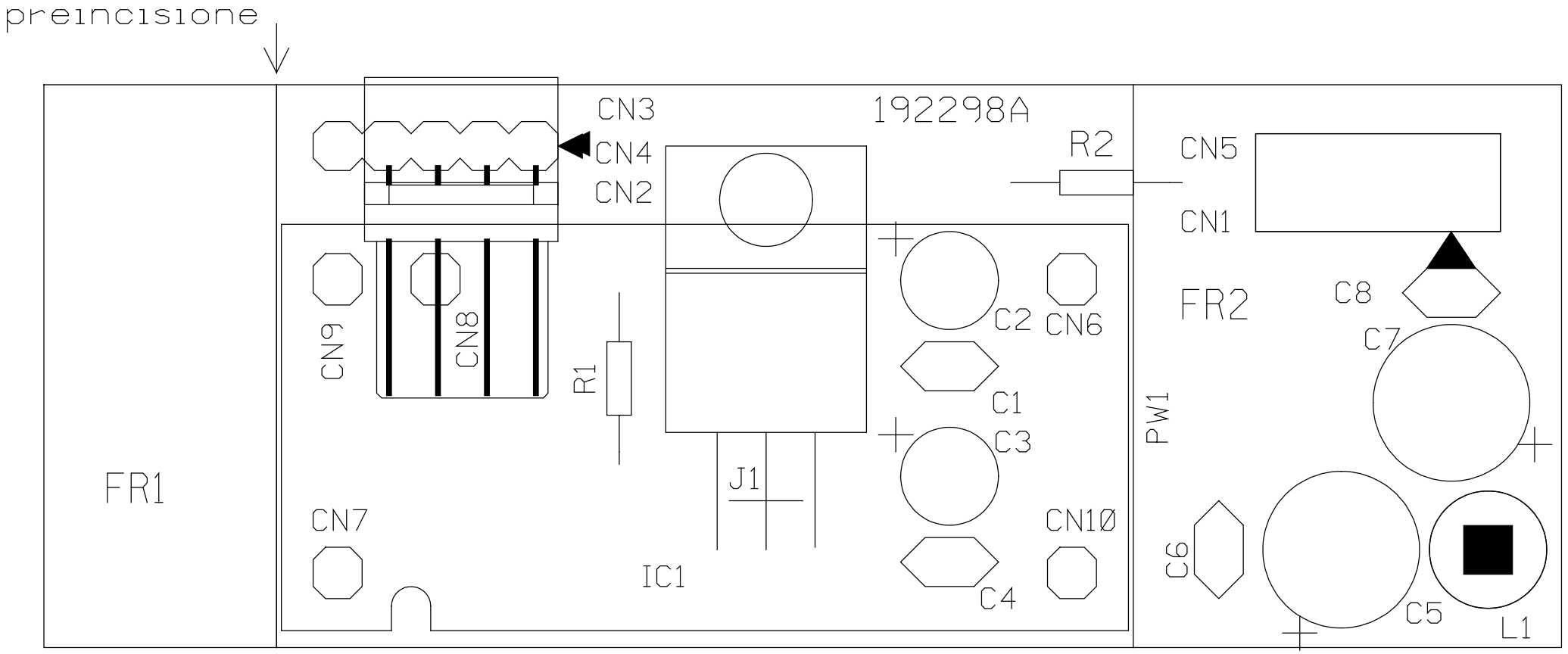
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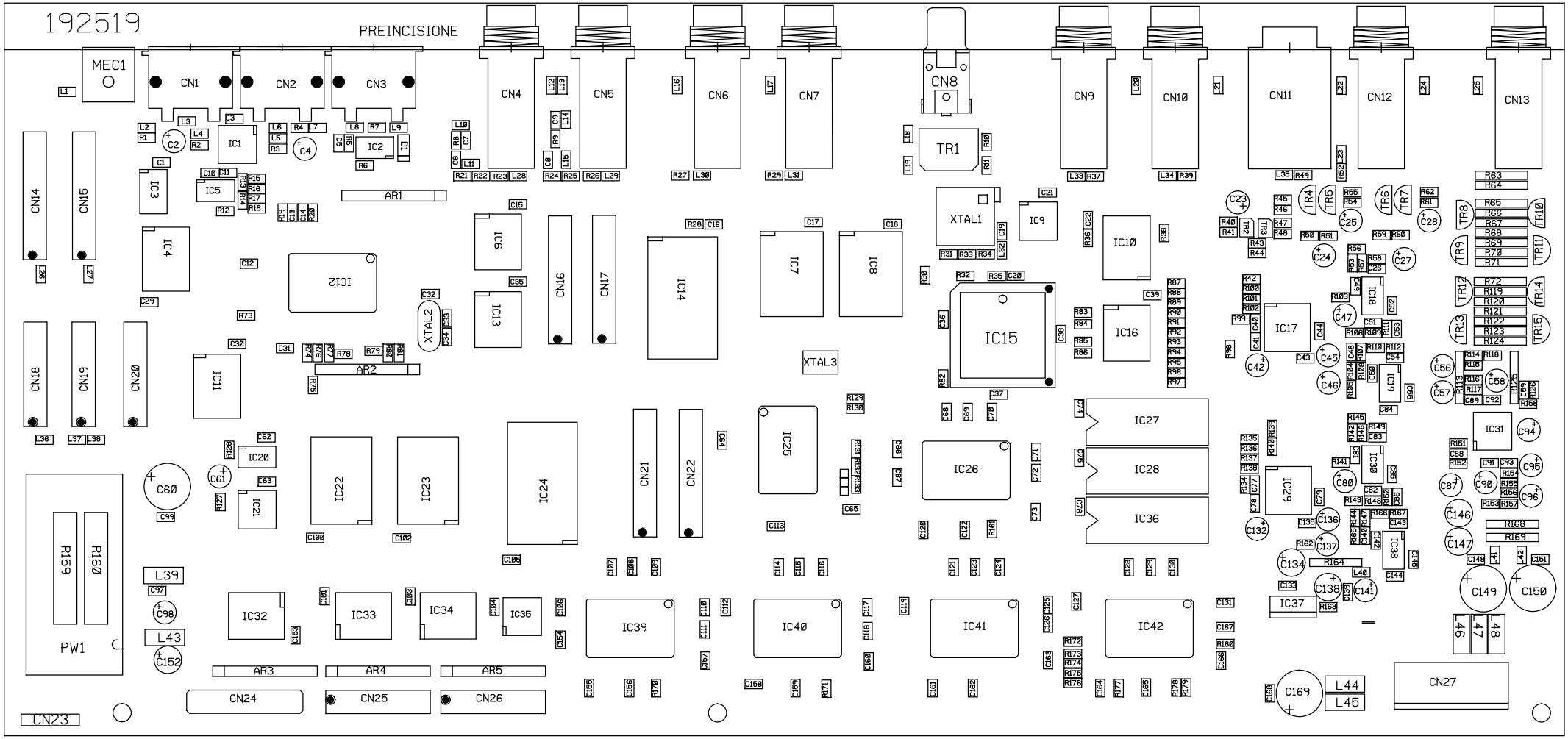
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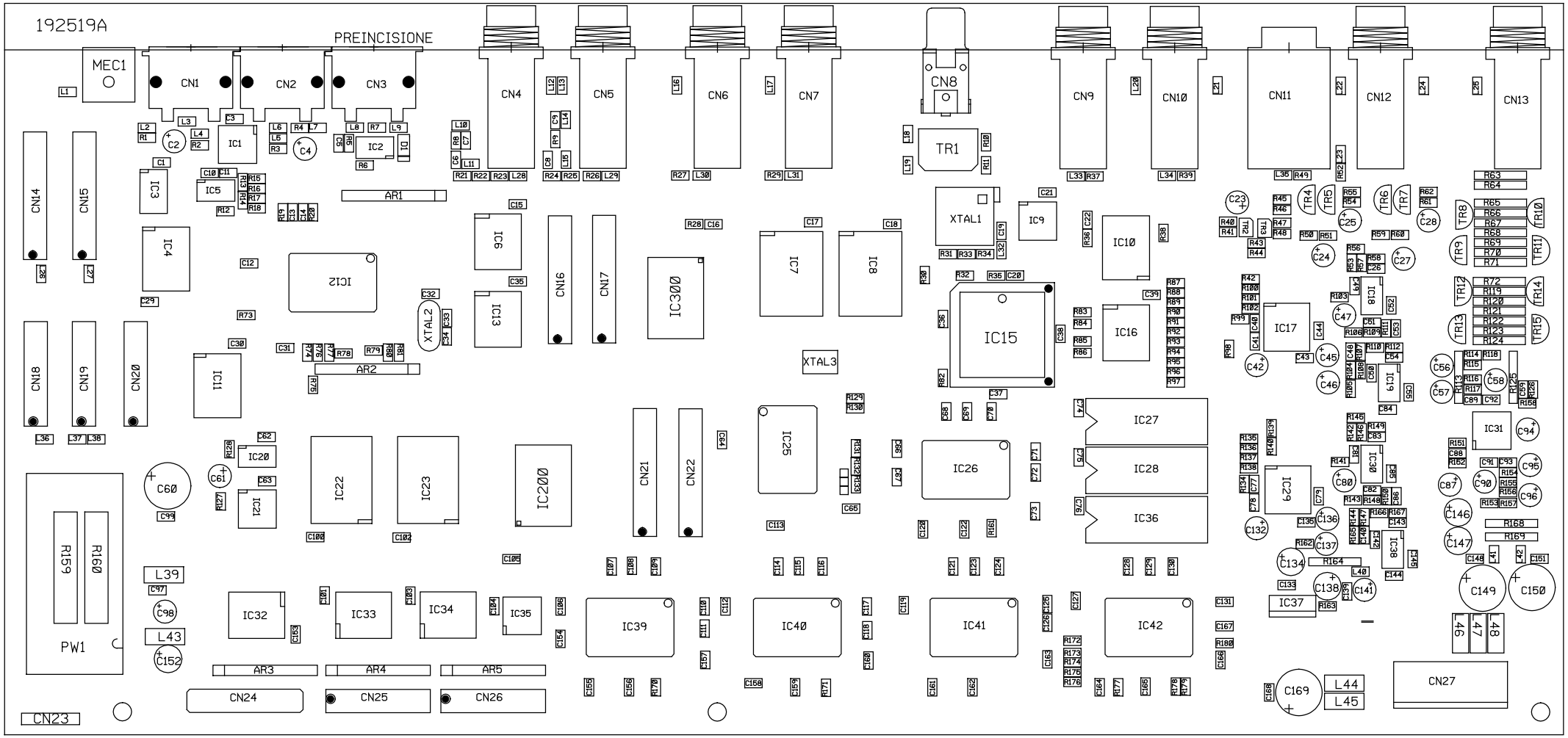
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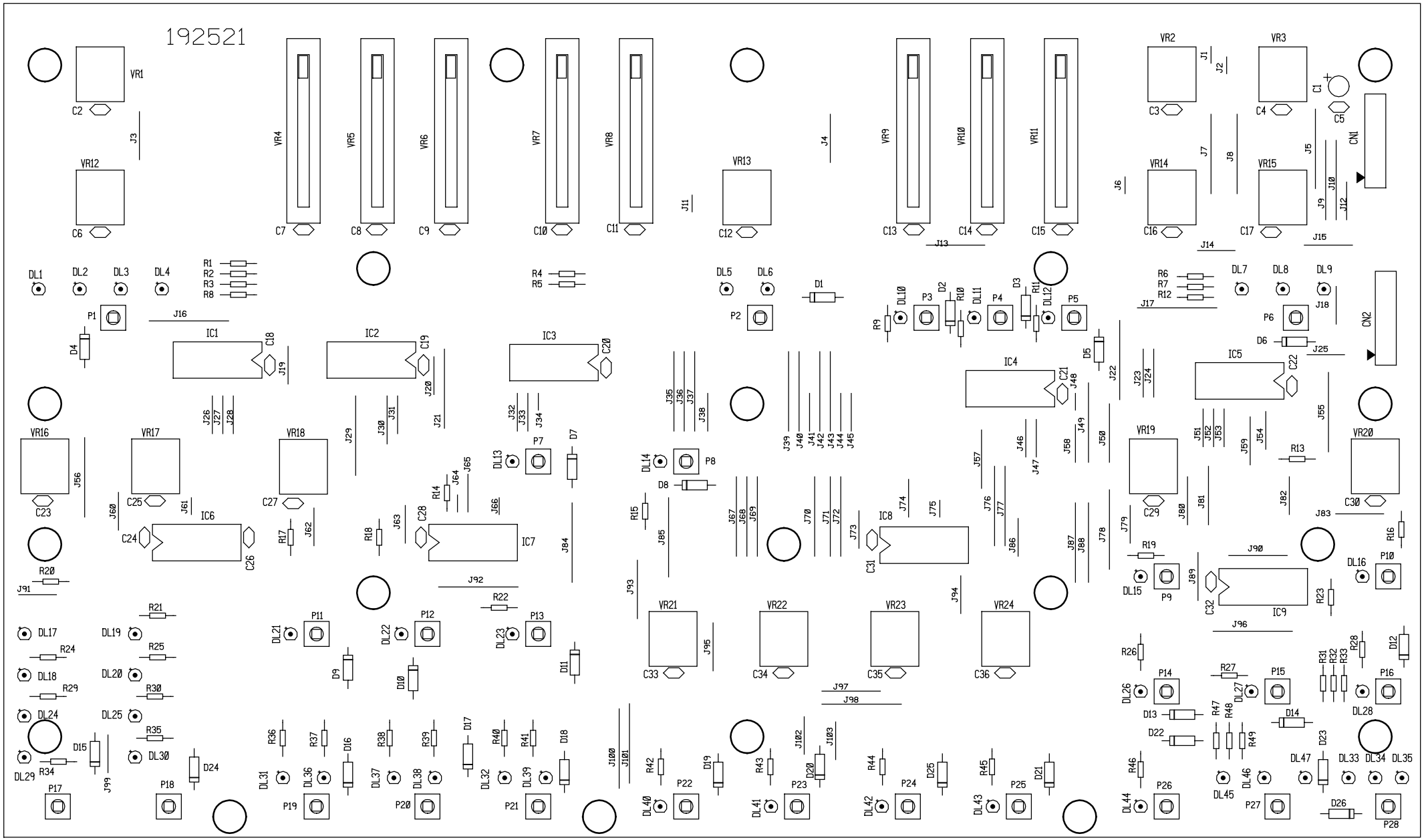
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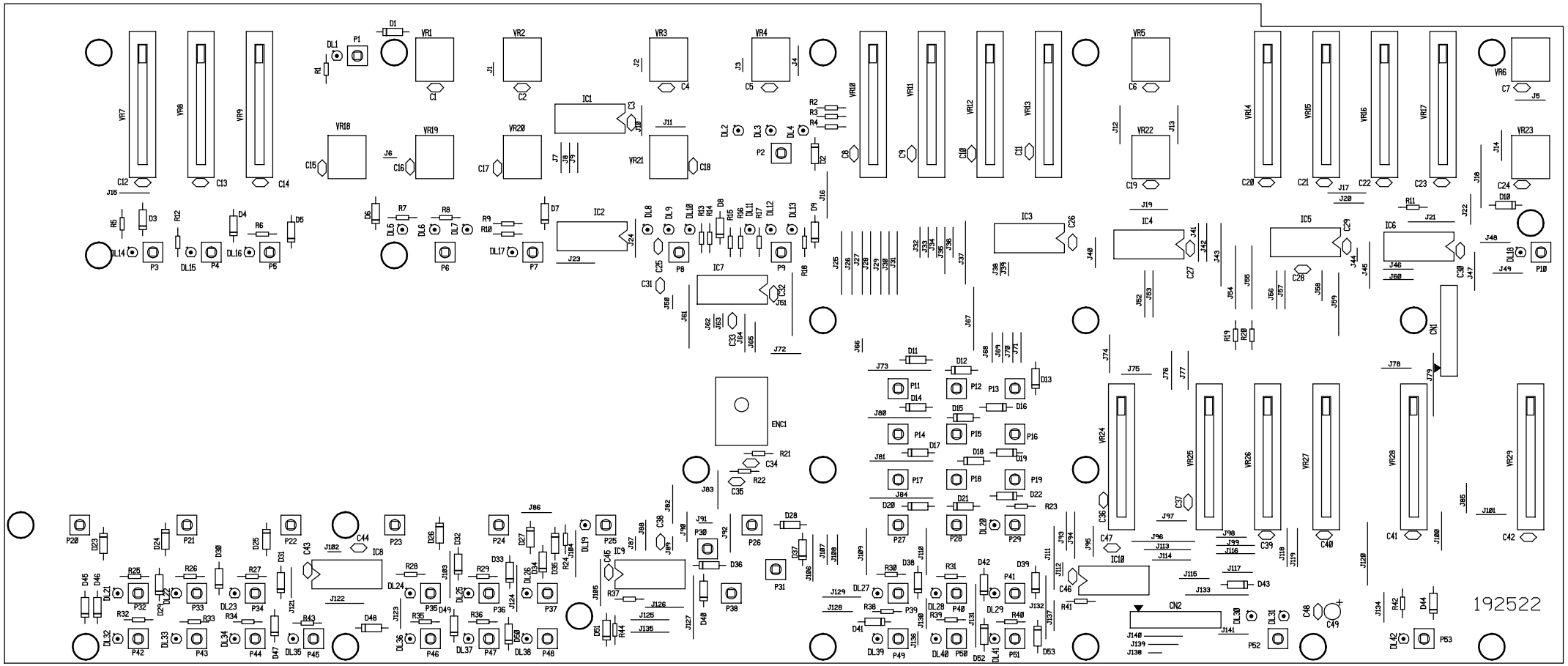
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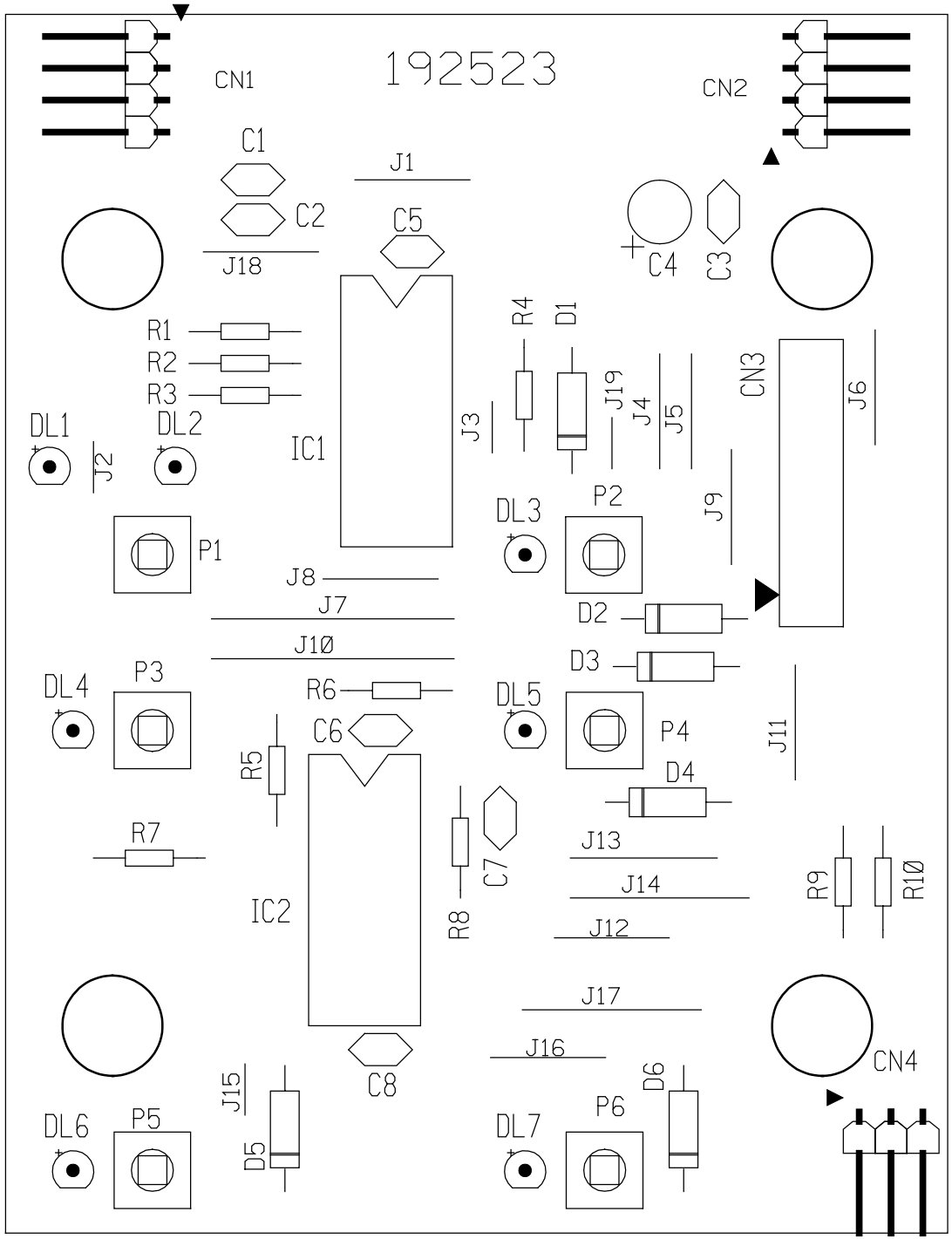
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Oberheim.